Simultaneous Driver and Wire Sizing for Performance and Power Optimization

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Abstract

In this paper, we study the *simultaneous driver and wire sizing (SDWS) problem* under two objective functions: (i) delay minimization only, or (ii) combined delay and power dissipation minimization. We present general formulations of the SDWS problem under these two objectives based on the distributed Elmore delay model with consideration of both capacitive power dissipation and short-circuit power dissipation. We show several interesting properties of the optimal SDWS solutions under the two objectives, including an important result (Theorem 5) which reveals the relationship between driver sizing and optimal wire sizing. These results lead to polynomial time algorithms for computing the lower and upper bounds of optimal SDWS solutions under the two objectives, and efficient algorithms for computing optimal SDWS solutions under the two objectives. We have implemented these algorithms and compared them with existing design methods for driver sizing only or independent driver and wire sizing. Accurate SPICE simulation shows that our methods reduce the delay by up to 12%–49% and power dissipation by 26%–63% compared with existing design methods.

1 Introduction

Delay minimization and power dissipation minimization are two important objectives in the design of the high-performance, portable, and wireless computing and communication systems. We believe that both device design (i.e. transistor/cell design) and interconnect design have to be considered and optimized simultaneously in order to achieve these two objectives. This new design methodology is especially important as the VLSI fabrication technology advances to submicron device dimension and gigahertz clock frequency. In this case, interconnect delay becomes an important factor in determining circuit speed, the *distributed* nature of the interconnect structure must be considered, and the capacitive power dissipation on charging/discharging interconnect structures takes a significant portion of overall system power. The objective of this paper is to study the simultaneous driver and wire sizing problem for both delay and power optimization.

In the past, two methods are commonly used to improve the performance of long interconnect lines. One method is driver sizing, which uses a large driver or a series of cascaded drivers of increasing sizes to drive long interconnect lines [2]. Another method is to break long interconnect lines into shorter segments by inserting repeaters. These repeaters can also be sized properly for further reduction in interconnect delay [2]. Both methods are effective for interconnect delay reduction but with substantial increase in power consumption.

Recent studies show that interconnect delay can also be reduced by interconnect topology optimization and wiresizing optimization. A number of interconnect topologies have been proposed for interconnect performance optimization, including bounded-radius bounded-cost trees [7], AHHK trees [1], maximum performance trees [6], A-trees [9], low-delay trees [3], and IDW/CFD trees [13]. Moreover, the wiresizing algorithm in [9, 10] can further minimize interconnect delay by optimally assigning different wire width to each wire segment in the interconnect design. Both interconnect topology optimization and wiresizing optimization are effective when resistance ratio, i.e. the driver resistance versus unit wire resistance, is small in the design [9].

Very recently, Cong, Koh and Leung [8] explored the possibility of both driver sizing and wire sizing. A simple heuristic algorithm was used to size drivers according to a fixed constant ratio, and an *independent* wire sizing optimization is performed for each driver sizing solution. Although encouraging experimental results were reported, it is not difficult to see that this method often produces sub-optimal solutions since driver sizing and wire sizing were carried out independently.

In this paper, we study the *simultaneous driver and wire sizing (SDWS) problem* under two objective functions: (i) delay minimization only, or (ii) combined delay and power dissipation minimization. We present general formulations of the SDWS problem under these two objectives based on the distributed Elmore delay model with consideration of both capacitive power dissipation and short-circuit power dissipation. We show several interesting properties of the optimal SDWS solutions under the two objectives, including an important result (Theorem 5) which reveals the relationship between driver sizing and optimal wire sizing. These results lead to polynomial time algorithms for computing the lower and upper bounds of the optimal SDWS solution under the two objectives, and efficient algorithms for computing optimal SDWS solutions under the two objectives. We have implemented these algorithms and compared them with existing design methods for driver sizing only or independent driver and wire sizing. Accurate SPICE simulation shows that our methods reduce

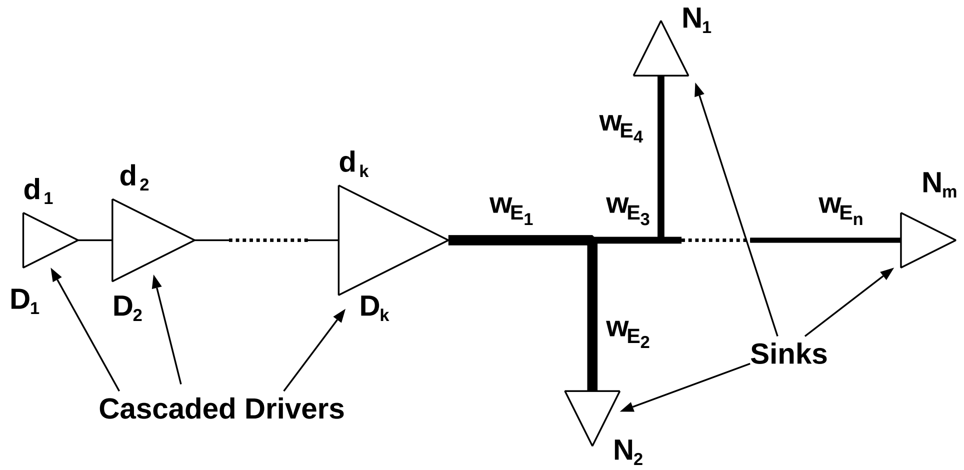

Figure 1: A k-stage cascaded drivers driving an interconnect tree T with sinks $\{N_1, N_2, \cdots, N_m\}$. w_{E_i} denotes the width of the wire segment E_i, $i = 1..n$ and d_i denotes the size of driver D_i at i-th stage, $i = 1..k$.

the delay by up to 12%–49% and power dissipation by 26%–63% compared with existing design methods. To the best of our knowledge, this is the first work which presents in-depth study of the SDWS problem for both delay and power optimization.

The remainder of this paper is organized as follows: In Section 2, we present the general formulation of the simultaneous driver sizing and wiresizing problems under the delay minimization objective and the combined delay and power minimization objective. In Section 3, we present results on optimal SDWS solutions for delay minimization. In Section 4, we present results on optimal SDWS solutions under the combined delay and power minimization objective. Section 5 shows the experimental results obtained by our SDWS algorithms and the comparative study with other existing methods. Section 6 concludes the paper with discussions of future work.

2 Problem Formulation

2.1 Performance Optimization

Assume that we are given a routing tree T implementing a signal net which consists of a source N_+, and a set of m sinks $\{N_1, N_2, \cdots, N_m\}$. A node in T refers to the source, or a sink, or a Steiner node, and a segment connects two nodes in T. Assume that $\{E_1, E_2, \cdots, E_n\}$ is the set of segments forming the tree T, where n is the total number of segments in the tree.

We assume that each wire segment has a set of discrete choices of wire widths $\{W_1, W_2, \cdots, W_r\}$ ($W_1 < W_2 < \cdots < W_r$). We use w_{E_i} to denote the width of the wire segment E_i, $i = 1..n$.

Furthermore, we assume that the signal net is driven by a chain of cascaded drivers of k stages at the source as shown in Figure 1. We use $\mathcal{D} = \{d_1, d_2, \cdots, d_k\}$ to denote a driver sizing solution, where d_i denotes the size of driver D_i at i-th stage ($i = 1..k$). We assume that driver D_1 is of minimum size, i.e. $d_1 = 1$. Given the

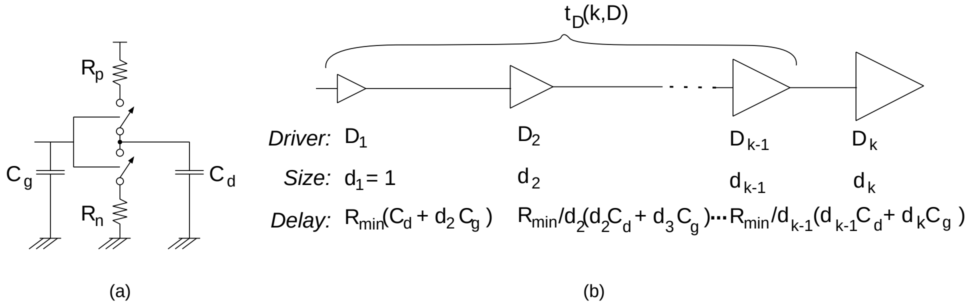

Figure 2: (a) A switch-level RC model of a driver (b) Inter-stage delay of a k-stage cascaded drivers until the gate of the k-th driver.

above definitions, the problem of simultaneous driver and wire sizing (SDWS) for performance optimization can be defined as follows:

Formulation 1 *Given a routing tree T, the SDWS problem for delay minimization (SDWS-D) is to determine the number of stages k, a driver sizing solution $\mathcal{D}$, and a wiresizing solution $\mathcal{W}$ on T, such that the performance measure $t(T,k,\mathcal{D},\mathcal{W})$ is optimized.*

If we fix the number of stages k, a restricted version of the SDWS-D problem called the *k-SDWS-D* problem can be defined as follows: Given a routing tree T and a chain of k drivers, the k-SDWS-D problem is to determine the optimal driver and wire sizing solution $\mathcal{D}$ and $\mathcal{W}$, such that the performance measure $t(T,k,\mathcal{D},\mathcal{W})$ is optimized.

The performance measure $t(T,k,\mathcal{D},\mathcal{W})$ approximates the delay of the signal net from the source to one or several critical sinks, and it can be decomposed as follows:

$$t(T,k,\mathcal{D},\mathcal{W}) \quad = \quad t_D(k,\mathcal{D}) + t_I(T,k,\mathcal{D},\mathcal{W}) \tag{1}$$

where the first term $t_D(k,\mathcal{D})$ measures the delay due to the drivers and the second term $t_I(T,k,\mathcal{D},\mathcal{W})$ measures the interconnect delay. We estimate $t_D(k,\mathcal{D})$ based on a switch-level RC model of drivers. The interconnect delay $t_I(T,k,\mathcal{D},\mathcal{W})$ is measured by the distributed Elmore delay model [12].

2.1.1 RC Delay Model for Drivers

We estimate the delays of the drivers based on a switch-level RC model of drivers. Figure 2(a) shows a minimum-size inverter (driver) with a p-transistor resistance R_p and a n-transistor resistance R_n. We assume that $R_p = R_n = R_{min}$. Let C_g denote the gate capacitance and C_d denote the capacitance due to the source and drain diffusion of the minimum-size driver.

Figure 2(b) illustrates the delay due to a sequence of k cascaded drivers $\mathcal{D}$. The delay from driver D_i to D_{i+1} $(1 \le i \le k-1)$ is the product of the resistance of D_i and its capacitive load:

$$\frac{R_{min}}{d_i} \cdot (C_d \cdot d_i + C_g \cdot d_{i+1}) = R_{min} \cdot C_d + R_{min} \cdot C_g \cdot \frac{d_{i+1}}{d_i} \tag{2}$$

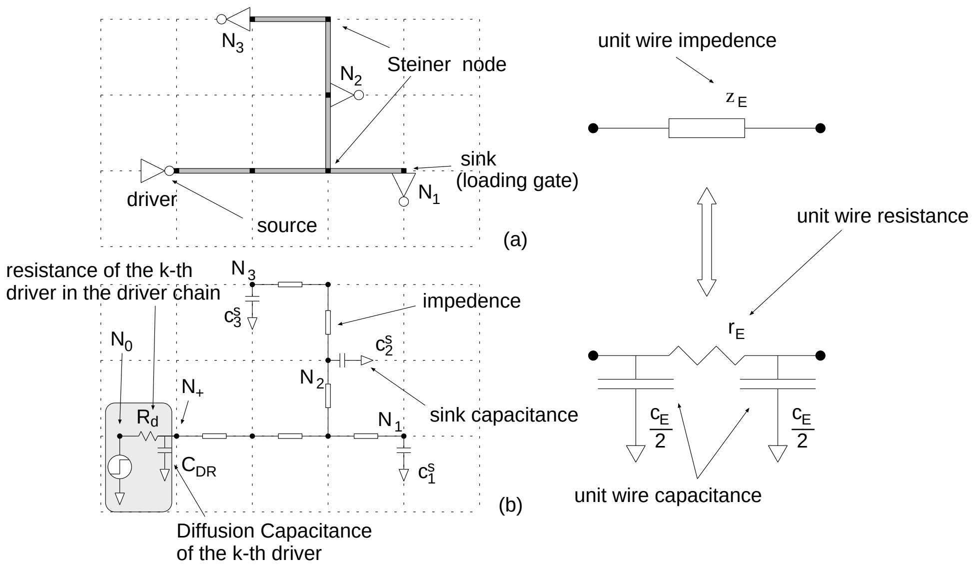

Figure 3: A uniform grid structure for the distributed RC interconnect model. (a) The layout of an interconnect tree T with 3 sinks N_1, N_2, and N_3. (b) The corresponding distributed RC interconnect model of T. Each grid edge E in T connecting two adjacent nodes is modeled as a π-type RC circuit containing a resistor of r_E and two capacitors of $\frac{c_E}{2}$ each. Each sink has an extra loading capacitance.

The total delay up to the gate of the last driver $t_D(k, \mathcal{D})$ (excluding the last driver) can be expressed as follows:

$$\begin{aligned} t_D(k,\mathcal{D}) &= (k-1)\cdot R_{min}\cdot C_d + \sum_{i=1}^{k-1} \frac{R_{min}\cdot C_g \cdot d_{i+1}}{d_i} \\ &= \mathcal{J}_1 + \mathcal{J}_2 \cdot \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \qquad (3) \end{aligned}$$

where $\mathcal{J}_1 = (k-1)\cdot R_{min}\cdot C_d$, and $\mathcal{J}_2 = R_{min}\cdot C_g$. Notice that delay through the k-th driver will be counted as part of interconnect delay in Section 2.1.3.

2.1.2 Distributed Elmore Delay Model for Interconnect

We use the distributed Elmore delay model [12] for interconnect delay measure. The formulations used in this section are based on those in [10]. In order to model a routing tree as a distributed RC circuit accurately, a uniform grid structure is superimposed on the routing plane, and each wire segment in the routing plane is divided into a sequence of wires of unit length as shown in Figure 3. In this case, T consists of a set of unit-length wire segments, each may have a different width[1].

For each edge E in the tree T, we use a π-type RC circuit to model E, where r_E and c_E are the interconnect resistance and capacitance respectively. Given an edge E, we use w_E to denote the width of the grid edge E. Assume that a unit-width unit-grid-length wire has wire resistance r_0, wire area capacitance c_0 and wire fringing

[1] In [9, 10], a segment in T is defined to be an edge in the rectilinear Steiner tree. In that case, segments in T are of different lengths, and the wire width is uniform within each segment.

capacitance c_1, then $r_E = \frac{r_0}{w_E}$ and $c_E = c_0 \cdot w_E + c_1$ for any grid edge E. (Note that previous formulations in [9, 10] did not consider fringing effect. Also, c_1 can be used to represent mutual capacitance between adjacent wires in the same layer or adjacent layers, when it is known.)

We use c_u^s to denote the capacitance at sink u. To correctly model the driver resistance, we introduce an additional node N_0 and connect N_0 to N_+ via an additional segment with resistance $R_d = R_{min}/d_k$ and capacitance $C_{DR} = C_d \cdot d_k$ (the resistance and capacitance of the last driver in the cascaded driver chain) in the later discussions.

Given a grid edge E, we use $Des(E)$ to denote the set of grid edges in the subtree rooted at E (excluding E), and $Ans(E)$ to denote the set of grid edges $\{E' | E \in Des(E')\}$ (again, excluding E). That is, $Des(E)$ is the set of "descendant" grid edges of E, and $Ans(E)$ is the set of "ancestor" grid edges of E. Also, we use $sink(E)$ to denote the set of sinks in the subtree rooted at E, and C_E to denote the *total* capacitance in the subtree rooted at E (including both the wire capacitances and the sink capacitances). Furthermore, we use $sink(T)$ to denote the set of sinks in T and $P(u, v)$ to denote the unique path from u to v for any grid points u, v in the routing tree.

We use the Elmore delay model [12] as the objective function for delay optimization. Given a distributed RC circuit tree T, the signal delay at a particular node N_i, denoted as $t(N_i)$, is computed as follows:

$$t(N_i) = \sum_{u \in P(N_0, N_i)} r_u \cdot (\frac{c_u}{2} + C_u) \tag{4}$$

where the summation is taken over all the grid points on the path from the driver N_0 to the node N_i.

2.1.3 Single Critical Sink Formulation

We first study the case where there is only one critical sink N_i in the net. Let R_d and C_{DR} be the resistance and diffusion capacitance of the last driver in the driver chain respectively, i.e. $R_d = R_{min}/d_k$, $C_{DR} = C_d \cdot d_k$. Also, we use $C_{IL}(T, \mathcal{W})$ to denote total capacitance of interconnect tree T (including the loading capacitance at the sinks). We define

$$C_{IL}(T, \mathcal{W}) = \sum_{u \in sink(T)} c_u^s + c_0 \cdot \sum_{E \in T} w_E + \sum_{E \in T} c_1 \tag{5}$$

which is the total capacitance that the driver chain will drive. According to Eqn. (4) and following a similar derivations in [9, 10], the signal delay $t_i(T, R_d, \mathcal{W})$ at N_i under a given wiresizing solution $\mathcal{W}$ is:

$$\begin{aligned}
& t_i(T, R_d, \mathcal{W}) \\
= \; & R_d \cdot (C_{DR} + C_{IL}(T, \mathcal{W})) \; + \sum_{E \in P(N_+, N_i)} r_E \cdot (\frac{c_E}{2} + C_E) \\
= \; & \left\{ R_d \cdot C_{DR} \; + \; R_d \cdot \sum_{u \in sink(T)} c_u^s \; + \; R_d \cdot c_0 \cdot \sum_{E \in T} w_E + R_d \cdot \sum_{E \in T} c_1 \right\} + \\
& \left\{ \sum_{E \in P(N_+, N_i)} \frac{r_0}{w_E} \cdot \frac{c_0 \cdot w_E + c_1}{2} \; + \sum_{E \in P(N_+, N_i)} \frac{r_0}{w_E} \cdot C_E \right\}
\end{aligned}$$

$$
\begin{aligned}
&= R_d \cdot C_{DR} + R_d \cdot \sum_{u \in sink(T)} c^s_u + R_d \cdot c_0 \cdot \sum_{E \in T} w_E + R_d \cdot \sum_{E \in T} c_1 + \left\{ \sum_{E \in P(N_+, N_i)} \frac{r_0 \cdot c_0}{2} + \right. \\
&\quad \left. \sum_{E \in P(N_+, N_i)} \frac{r_0 \cdot c_1}{2 \cdot w_E} \right\} + \left\{ \sum_{E \in P(N_+, N_i)} \frac{r_0}{w_E} \cdot \sum_{E' \in Des(E)} (c_0 \cdot w_{E'} + c_1) + \sum_{E \in P(N_+, N_i)} \frac{r_0}{w_E} \cdot \sum_{v \in sink(E)} c^s_v \right\} \\
&= R_d \cdot C_{DR} + R_d \cdot \sum_{u \in sink(T)} c^s_u + R_d \cdot c_0 \cdot \sum_{E \in T} w_E + R_d \cdot \sum_{E \in T} c_1 + \sum_{E \in P(N_+, N_i)} \frac{r_0 \cdot c_0}{2} + \\
&\quad \frac{r_0 \cdot c_1}{2} \cdot \sum_{E \in P(N_+, N_i)} \frac{1}{w_E} + \left\{ r_0 \cdot c_0 \cdot \sum_{E \in P(N_+, N_i)} \sum_{E' \in Des(E)} \frac{w_{E'}}{w_E} + \right. \\
&\quad \left. r_0 \cdot c_1 \cdot \sum_{E \in P(N_+, N_i)} \sum_{E' \in Des(E)} \frac{1}{w_E} \right\} + r_0 \cdot \sum_{E \in P(N_+, N_i)} \sum_{v \in sink(E)} c^s_v \cdot \frac{1}{w_E} \qquad (6)
\end{aligned}
$$

Let

$$
\begin{aligned}
\mathcal{K}^i_0 &= R_d \cdot C_{DR} + R_d \cdot \sum_{u \in sink(T)} c^s_u + R_d \cdot \sum_{E \in T} c_1 + \sum_{E \in P(N_+, N_i)} \frac{r_0 \cdot c_0}{2} \\
\mathcal{K}_1 &= R_d \cdot c_0 \\
\mathcal{K}_2 &= r_0 \cdot c_0 \\
\mathcal{K}_3 &= r_0 \cdot c_1 \\
\mathcal{K}_4 &= r_0 \\
\mathcal{K}_5 &= \frac{r_0 \cdot c_1}{2} \qquad (7)
\end{aligned}
$$

Note that given a fixed R_d, $\mathcal{K}^i_0$ is a constant with respect to the timing-critical sink N_i and $\mathcal{K}_1$ to $\mathcal{K}_5$ are all constant depending only on the technology. Also, we define the functions $f_i(E, E')$, $g_i(E)$ and $h_i(E)$ as follows:

$$
\begin{aligned}
f_i(E, E') &= \begin{cases} 1 & \text{if } E \in P(N_+, N_i) \text{ and } E' \in Des(E) \\ 0 & \text{otherwise} \end{cases} \\
g_i(E) &= \begin{cases} \sum_{v \in sink(E)} c^s_v & \text{if } E \in P(N_+, N_i) \\ 0 & \text{otherwise} \end{cases} \\
h_i(E) &= \begin{cases} 1 & \text{if } E \in P(N_+, N_i) \\ 0 & \text{otherwise} \end{cases}
\end{aligned}
$$

Note that $h_i(E) = f_i(E, E')$ for all $E' \in Des(E)$.

Rearranging, we can rewrite Eqn. (6) as follows:

$$
\begin{aligned}
t_i(T, R_d, \mathcal{W}) &= \mathcal{K}^i_0 + \mathcal{K}_1 \cdot \sum_{E \in T} w_E + \mathcal{K}_2 \cdot \sum_{E, E' \in T} f_i(E, E') \cdot \frac{w_{E'}}{w_E} + \mathcal{K}_3 \cdot \sum_{E, E' \in T} f_i(E, E') \cdot \frac{1}{w_E} + \\
&\quad \mathcal{K}_4 \cdot \sum_{E} g_i(E) \cdot \frac{1}{w_E} + \mathcal{K}_5 \cdot \sum_{E \in T} h_i(E) \cdot \frac{1}{w_E} \qquad (8)
\end{aligned}
$$

2.1.4 Multiple Critical Sinks Formulation

Let $sink(T)$ denote the set of sinks in T. When there are several critical sinks of different priorities in the routing tree, the previous formulation can be generalized as follows:

$$t(T, R_d, \mathcal{W}) = \sum_{N_i \in sink(T)} \lambda_i \cdot t_i(T, R_d, \mathcal{W}) \tag{9}$$

where λ_i is the weight of the delay penalty to sink N_i. The larger λ_i is, the more critical sink N_i is. We normalize λ_i's such that $\sum_{N_i \in sink(T)} \lambda_i = 1$. We can rewrite Eqn. (9) as follows:

$$\begin{aligned}
t(T, R_d, \mathcal{W}) &= \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_0^i + \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_1 \cdot \sum_{E \in T} w_E + \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_2 \cdot \sum_{E,E' \in T} f_i(E,E') \cdot \frac{w_{E'}}{w_E} + \\
&\quad \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_3 \cdot \sum_{E,E' \in T} f_i(E,E') \cdot \frac{1}{w_E} + \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_4 \cdot \sum_{E,E' \in T} g_i(E) \cdot \frac{1}{w_E} + \\
&\quad \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_5 \cdot \sum_{E \in T} h_i(E) \cdot \frac{1}{w_E} \\
&= \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_0^i + \mathcal{K}_1 \cdot \sum_{E \in T} w_E + \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} \frac{w_{E'}}{w_E} \cdot \left\{ \sum_{N_i \in sink(T)} \lambda_i \cdot f_i(E,E') \right\} + \\
&\quad \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} \frac{1}{w_E} \cdot \left\{ \sum_{N_i \in sink(T)} \lambda_i \cdot f_i(E,E') \right\} + \mathcal{K}_4 \cdot \sum_{E \in T} \frac{1}{w_E} \cdot \left\{ \sum_{N_i \in sink(T)} \lambda_i \cdot g_i(E) \right\} + \\
&\quad \mathcal{K}_5 \cdot \sum_{E \in T} \frac{1}{w_E} \cdot \left\{ \sum_{N_i \in sink(T)} \lambda_i \cdot h_i(E) \right\} \\
&= \mathcal{K}_0 + \mathcal{K}_1 \cdot \sum_{E \in T} w_E + \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{w_{E'}}{w_E} + \\
&\quad \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} + \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} + \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E}
\end{aligned} \tag{10}$$

where

$$\begin{aligned}
\mathcal{K}_0 &= \sum_{N_i \in sink(T)} \lambda_i \cdot \mathcal{K}_0^i \\
F(E,E') &= \sum_{N_i \in sink(T)} \lambda_i \cdot f_i(E,E') \\
G(E) &= \sum_{N_i \in sink(T)} \lambda_i \cdot g_i(E) \\
H(E) &= \sum_{N_i \in sink(T)} \lambda_i \cdot h_i(E)
\end{aligned} \tag{11}$$

A careful study of F's, G's and H's reveals the following properties:

$$\begin{aligned}
F(E_1, E_2) &\geq F(E_1, E_2') && \text{if } E_2 \in Des(E_2') \\
F(E_1, E_2) &\geq F(E_1', E_2) && \text{if } E_1 \in Ans(E_1') \\
G(E_1) &\geq G(E_1') && \text{if } E_1 \in Ans(E_1') \\
H(E_1) &\geq H(E_1') && \text{if } E_1 \in Ans(E_1') \\
H(E_1) &= F(E_1, E_2) && \text{if } E_2 \in Ans(E_1)
\end{aligned} \tag{12}$$

2.1.5 Performance Optimization Objective of the SDWS Problem

Let $t_I(T, k, \mathcal{D}, \mathcal{W}) = t(T, R_d, \mathcal{W})$. Hence, the performance measure on both driver and interconnect delay $t(T, k, \mathcal{D}, \mathcal{W})$ in Eqn. (1) can be written as

$$\begin{aligned} t(T,k,\mathcal{D},\mathcal{W}) &= t_D(k,\mathcal{D}) + t_I(T,k,\mathcal{D},\mathcal{W}) \\ &= \left\{ \mathcal{J}_1 + \mathcal{J}_2 \cdot \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \right\} + \left\{ \mathcal{K}_0 + \mathcal{K}_1 \cdot \sum_{E \in T} w_E + \right. \\ & \quad \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{w_{E'}}{w_E} + \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} + \\ & \quad \left. \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} + \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \right\} \end{aligned} \tag{13}$$

where $\mathcal{K}_0$, $\mathcal{K}_1$, $\mathcal{K}_2$, $\mathcal{K}_3$, $\mathcal{K}_4$ and $\mathcal{K}_5$ are constants defined in Eqn. (7) and (11).

2.2 Performance and Power Optimization

Driver and wire sizing are effective approaches to reduce interconnect delay. However, larger driver size and additional routing capacitance also increases the power dissipation. In practice, high-speed circuit design requires a careful tradeoff between performance and power. We define the SDWS problem for both delay and power optimization (SDWS-DP) as follows:

Formulation 2 *Given a routing tree T, the SDWS problem for both delay and power optimization (SDWS-DP) is to determine the number of stages k, a driver sizing solution $\mathcal{D}$, and a wiresizing solution $\mathcal{W}$ on T, such that the performance measure $obj(T, k, \mathcal{D}, \mathcal{W})$ defined below is minimized:*

$$obj(T,k,\mathcal{D},\mathcal{W}) = \alpha \cdot Power(T,k,\mathcal{D},\mathcal{W}) \; + \; \gamma \cdot t(T,k,\mathcal{D},\mathcal{W}) \tag{14}$$

where $t(T, k, \mathcal{D}, \mathcal{W})$ is the performance measure and $Power(T, k, \mathcal{D}, \mathcal{W})$ is the power dissipation, α and γ are adjustable non-negative parameters controlling the trade-off between performance and power dissipation.

Similarly, if we fix the number of stages k, we can define the *k-SDWS-DP* problem as follows: Given a routing tree T and a chain of k drivers, determine the optimal driver and wire sizing solution $\mathcal{D}$ and $\mathcal{W}$, such that the performance measure $obj(T, k, \mathcal{D}, \mathcal{W})$ is minimized.

2.2.1 Power Dissipation Formulation

There are two components that determine the amount of power dissipated in a CMOS circuit, namely, *static* dissipation due to leakage current, and *dynamic* dissipation due to switching transient current (short-circuit dissipation) and charging and discharging of load capacitances (capacitive dissipation) [16]. We consider only dynamic dissipation in our formulation since static dissipation is usually 2 to 3 order of magnitude smaller. Given a loading capacitance C_L, we can write the capacitive and short-circuit dissipation of a single driver as follows [16]:

$$Power_{cap} = f \cdot C_L \cdot V_{dd}^2 \tag{15}$$

$$Power_{sc} \;=\; f \cdot \frac{\beta}{12} \cdot (V_{dd} - 2V_t)^3 \cdot t_{rf} \tag{16}$$

where f is the switching frequency of the input signal, β is the MOS transistor gain factor, V_t is the threshold voltage and t_{rf} is the rise and fall time of the input signal which are assumed to be equal.

Consider a chain of k drivers. For driver D_i ($i = 1..k-1$), the capacitive load of the driver is assumed to be the sum of its diffusion capacitance $C_d \cdot d_i$ and the gate capacitance $C_g \cdot d_{i+1}$ of the next driver D_{i+1}. The last driver D_k has a capacitive load of $C_d \cdot d_k + C_{IL}(T, \mathcal{W})$. Hence the capacitive power of the cascaded drivers is

$$\begin{aligned} Power_{cap}(k, \mathcal{D}, C_{IL}(T, \mathcal{W})) &= f \cdot V_{dd}^2 \cdot \left(C_d \;+\; \sum_{i=2}^{k-1} (d_i \cdot C_d + d_{i+1} \cdot C_g) \;+\; d_k \cdot C_d \;+\; C_{IL}(T, \mathcal{W}) \right) \\ &= \mathcal{L}_0 \;+\; \mathcal{L}_1 \cdot \left(\sum_{i=2}^{k} d_i \;+\; \frac{C_{IL}(T, \mathcal{W})}{C_g + C_d} \right) \end{aligned} \tag{17}$$

where $\mathcal{L}_0 = f \cdot V_{dd}^2 \cdot C_d$ and $\mathcal{L}_1 = f \cdot V_{dd}^2 \cdot (C_g + C_d)$.

Let β_{min} be the gain factor of a minimum-size driver. The gain factor of a driver of size d can be defined as $d \cdot \beta_{min}$. Hence, we can write the short-circuit power of the cascaded drivers as follows [16]:

$$\begin{aligned} Power_{sc}(k, \mathcal{D}, C_{IL}(T, \mathcal{W})) &= f \cdot \sum_{i=1}^{k} \frac{\beta_{min} \cdot d_i}{12} \cdot (V_{dd} - 2V_t)^3 \cdot t_{rf} \\ &= \mathcal{L}_2 \cdot \sum_{i=1}^{k} d_i \\ &= \mathcal{L}_2 \;+\; \mathcal{L}_2 \cdot \sum_{i=2}^{k} d_i \end{aligned} \tag{18}$$

where $\mathcal{L}_2 = f \cdot \frac{\beta_{min}}{12} \cdot (V_{dd} - V_t)^3 \cdot t_{rf}$.

Summing up the capacitive and short-circuit power, the dynamic power dissipation of the circuit can be written as:

$$\begin{aligned} Power(T, k, \mathcal{D}, \mathcal{W}) &= Power_{cap}(k, \mathcal{D}, C_{IL}(T, \mathcal{W})) \;+\; Power_{sc}(k, \mathcal{D}, C_{IL}(T, \mathcal{W})) \\ &= \left\{ \mathcal{L}_0 \;+\; \mathcal{L}_1 \cdot (\sum_{i=2}^{k} d_i + \frac{C_{IL}(T, \mathcal{W})}{C_g + C_d}) \right\} \;+\; \left\{ \mathcal{L}_2 \;+\; \mathcal{L}_2 \cdot \sum_{i=2}^{k} d_i \right\} \\ &= \mathcal{L}_0 \;+\; \mathcal{L}_1 \cdot \frac{C_{IL}(T, \mathcal{W})}{C_g + C_d} + \mathcal{L}_2 + (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \end{aligned} \tag{19}$$

2.2.2 Trade-Off Between Performance and Power

We can now write the trade-off between performance and power in Eqn. (14) as follows:

$$\begin{aligned} obj(T, k, \mathcal{D}, \mathcal{W}) &= \alpha \cdot Power(T, k, \mathcal{D}, \mathcal{W}) \;+\; \gamma \cdot t(T, k, \mathcal{D}, \mathcal{W}) \\ &= \left\{ \alpha \cdot \left(\mathcal{L}_0 \;+\; \mathcal{L}_1 \cdot \frac{C_{IL}(T, \mathcal{W})}{C_g + C_d} + \mathcal{L}_2 + (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \right) \right\} \;+\; \left\{ \gamma \cdot \left(\mathcal{J}_1 \;+\; \mathcal{J}_2 \cdot \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \;+ \right.\right. \\ &\quad \mathcal{K}_0 \;+\; \mathcal{K}_1 \cdot \sum_{E \in T} w_E \;+\; \mathcal{K}_2 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot \frac{w_{E'}}{w_E} \;+ \end{aligned}$$

$$\mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} \ + \ \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} \ + $$
$$\mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \Bigg) \Bigg\} \tag{20}$$

There are two terms that links the driver chain and the interconnect in both the power formula and delay formula, namely the last driver d_k and the capacitive load $C_{IL}(T, \mathcal{W})$. Suppose a wire-width assignment $\mathcal{W}$ is given for a routing tree T, the capacitive load $C_{IL}(T, \mathcal{W})$ can be computed. The drivers are sized to minimize the following:

$$\alpha \cdot \left(\mathcal{L}_0 \ + \ \mathcal{L}_1 \cdot \frac{C_{IL}(T,\mathcal{W})}{C_g + C_d} + \mathcal{L}_2 + (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \right) + \gamma \cdot \left\{ \mathcal{J}_1 + R_{min} \cdot C_d + \mathcal{J}_2 \cdot \left(\frac{C_{IL}(T,\mathcal{W})}{d_k \cdot C_g} \ + \ \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \right) \right\} \tag{21}$$

Eliminating the constant terms, minimizing the above formulation is equivalent to minimizing the following:

$$obj_{T,k,\mathcal{W}}(\mathcal{D}) = \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{C_{IL}(T,\mathcal{W})}{d_k \cdot C_g} \ + \ \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \right) \tag{22}$$

Given a driver size assignment, the wires are sized to minimize the following tradeoff between routing area and interconnect delay:

$$\begin{aligned}
& \alpha \cdot \mathcal{L}_1 \cdot \frac{C_{IL}(T,\mathcal{W})}{C_g + C_d} \ + \ \gamma \cdot t(T, R_d, \mathcal{W}) \\
= \ & \left\{ \alpha \cdot \mathcal{L}_1 \cdot \frac{1}{C_g + C_d} \cdot \left(\sum_{u \in sink(T)} c_u^s + c_0 \cdot \sum_{E \in T} w_E + \sum_{E \in T} c_1 \right) \right\} \ + \ \left\{ \gamma \cdot \Bigg(\mathcal{K}_0 \ + \ \mathcal{K}_1 \cdot \sum_{E \in T} w_E \ + \right. \\
& \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{w_{E'}}{w_E} \ + \ \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} \ + \ \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} \ + \\
& \left. \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \Bigg) \right\} \\
= \ & \left\{ \alpha \cdot \mathcal{L}_1 \cdot \frac{1}{C_g + C_d} \cdot \sum_{u \in sink(T)} c_u^s \ + \ \alpha \cdot \mathcal{L}_1 \cdot \frac{1}{C_g + C_d} \cdot \sum_{E \in T} c_1 \ + \ \gamma \cdot \mathcal{K}_0 \right\} \ + \\
& \left\{ (\alpha \cdot \mathcal{L}_1 \cdot \frac{1}{C_g + C_d} \cdot c_0 + \gamma \cdot \mathcal{K}_1) \cdot \sum_{E \in T} w_E \right\} \ + \ \left\{ \gamma \cdot \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{w_{E'}}{w_E} \right\} \ + \\
& \left\{ \gamma \cdot \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} \right\} \ + \ \left\{ \gamma \cdot \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} \right\} \ + \\
& \left\{ \gamma \cdot \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \right\}
\end{aligned} \tag{23}$$

The formulation is similar to Eqn. (10) except with difference in constant coefficients, which implies that the wiresizing results for delay minimization can also be applied to simultaneous power and performance optimization. After eliminating the constant terms, minimizing the above formula is equivalent to minimizing the following objective function:

$$obj_{T,k,\mathcal{D}}(\mathcal{W}) \ = \ (\alpha \cdot \mathcal{L}_1 \cdot \frac{1}{C_g + C_d} \cdot c_0 + \gamma \cdot \mathcal{K}_1) \cdot \sum_{E \in T} w_E \ + \ \gamma \cdot \mathcal{K}_2 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{w_{E'}}{w_E} \ +$$

$$\gamma \cdot \mathcal{K}_3 \cdot \sum_{E,E' \in T, E \neq E'} F(E,E') \cdot \frac{1}{w_E} \ + \ \gamma \cdot \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} \ + $$
$$\gamma \cdot \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \tag{24}$$

Since $Power(T,k,\mathcal{D},\mathcal{W})$ and $t(T,k,\mathcal{D},\mathcal{W})$ are usually of different orders of magnitude. The choice of α and γ in Eqn. (20) might be difficult. We find in our study that it is convenient to optimize the following objective:

$$obj(T,k,\mathcal{D},\mathcal{W}) \ = \ \alpha \cdot \frac{Power(T,k,\mathcal{D},\mathcal{W})}{Power_{min}(T)} \ + \ (1-\alpha) \cdot \frac{t(T,k,\mathcal{D},\mathcal{W})}{t_{min}(T,\mathcal{D},\mathcal{W})} \tag{25}$$

where $Power_{min}(T)$ is the minimum power required for driving an interconnect tree T and $t_{min}(T,\mathcal{D},\mathcal{W})$ is the minimum delay achievable by a chain of drivers driving an interconnect tree T.

Note that given a SDWS-DP problem, $Power_{min}(T)$ can be computed easily by assuming a single driver driving an interconnect tree where all interconnect grid edges are assigned with minimum wire width. On the other hand, $t_{min}(T,\mathcal{D},\mathcal{W})$ can be computed using the algorithms to be presented in Section 3. Therefore, they can be treated as constants. In this case, we can easily adjust parameter α between 0 and 1 to achieve smooth trade-off between performance and power.

3 Simultaneous Driver and Wire Sizing for Performance Optimization (SDWS-D Problem)

3.1 Properties of Optimal SDWS-D Solutions

We consider the simultaneous driver and wire sizing problem for performance optimization which minimizes the performance measure $t(T,k,\mathcal{D},\mathcal{W})$ specified by Eqn. (13). The lemmas and theorems in this subsection are used to prove the correctness of the bound computation algorithm and optimality of the optimal algorithm to the SDWS-P problem. If the reader is only interested to learn the algorithms, he/she may proceed directly to Section 3.2.

3.1.1 Properties of Optimal Driver Sizing Solutions for Performance Optimization

Theorem 1 *[16] Given the loading capacitance C_L, the number of stages k and the minimum gate capacitance C_g, the optimal stage ratio is $s = (\frac{C_L}{C_g})^{1/k}$.* □

3.1.2 Properties of Optimal Wire Sizing Solutions for Performance Optimization

The results in [10] showed several interesting properties of optimal wiresizing solutions for performance optimization, including the *separability*, the *monotone property*, and the *dominance property*. But they did not model the driver capacitance and interconnect fringing capacitance. Our study shows that these results still holds after we model the driver capacitance and fringing capacitance in interconnect delay formulation. Full proofs of these theorems are given in the Appendix at the end of this paper.

Theorem 2 (Separability): *If the width assignment of a path P originated from the source is given, the optimal width assignment for each subtree branching off from P can be carried out independently.* $\square$

Definition 1 *Given a routing tree T, a wiresizing solution $\mathcal{W}$ on T is a monotone assignment if $w_E \geq w_{E'}$ for any pair of segments E and E' such that $E \in Ans(E')$.*

Theorem 3 (Monotone Property): *For any given tree T, there exists a monotone optimal width assignment $\mathcal{W}^*$.* $\square$

Definition 2 *Given two wire width assignments $\mathcal{W}$ and $\mathcal{W}'$, $\mathcal{W}$* dominates *$\mathcal{W}'$ if for any segment E, the width assignment of E in $\mathcal{W}$ is greater than or equal to that of E in $\mathcal{W}'$.*

Definition 3 *Given a routing tree T, a wire width assignment $\mathcal{W}$ on T, and any particular segment $E \in T$, a* local refinement *on E is the operation to optimize the width of E based on the objective function in (10), without changing the width of other segments specified by $\mathcal{W}$.*

Theorem 4 (Dominance Property): *Given a routing tree T, let $\mathcal{W}^*$ be an optimal width assignment. If a width assignment $\mathcal{W}$ dominates $\mathcal{W}^*$, then a local refinement of $\mathcal{W}$ on any edge E in T still dominates $\mathcal{W}^*$. Similarly, if a width assignment $\mathcal{W}$ is dominated by $\mathcal{W}^*$, then a local refinement of $\mathcal{W}$ on any edge E in T is dominated by $\mathcal{W}^*$.* $\square$

3.1.3 Relation between Driver Sizing and Optimal Wire Sizing for Performance Optimization

Given a routing tree T with one or more critical sinks. Let R_d be the resistance of the last driver driving the routing tree and $\mathcal{W}^*$ be the corresponding optimal wire width assignment. Consider another chain of cascaded drivers such that R'_d is the resistance of the last driver and $\mathcal{W}'^*$ is the optimal wire width assignment. We shall show the following result that $R_d < R'_d$ implies that $\mathcal{W}^*$ dominates $\mathcal{W}'^*$ (Theorem 5):

Lemma 1 *If $R_d < R'_d$, then $area(\mathcal{W}^*) \geq area(\mathcal{W}'^*)$, where $area(\mathcal{W})$ denotes the total wire width used in wire width assignment $\mathcal{W}$.*

Proof: Let $\Delta t(T, R_d, \mathcal{W} \rightarrow \mathcal{W}')$ denote the difference $t(T, R_d, \mathcal{W}) - t(T, R_d, \mathcal{W}')$. Clearly, $\Delta t(T, R_d, \mathcal{W}^* \rightarrow \mathcal{W}'^*) \leq 0$ and $\Delta t(T, R'_d, \mathcal{W}'^* \rightarrow \mathcal{W}^*) \leq 0$ since $\mathcal{W}^*$ and $\mathcal{W}'^*$ are the optimal wiresizing solutions for R_d and R'_d, respectively. We can write $\Delta t(T, R_d, \mathcal{W}^* \rightarrow \mathcal{W}'^*)$ and $\Delta t(T, R'_d, \mathcal{W}'^* \rightarrow \mathcal{W}^*)$ as follows according to Eqn. (10):

$$\begin{aligned}
& \Delta t(T, R_d, \mathcal{W}^* \rightarrow \mathcal{W}'^*) \\
= \; & R_d \cdot c_0 \cdot \sum_{E \in T} (w^*_E - w'^*_E) \; + \; \mathcal{K}_2 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot \left(\frac{w^*_{E'}}{w^*_E} - \frac{w'^*_{E'}}{w'^*_E}\right) \; + \\
& \mathcal{K}_3 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot \left(\frac{1}{w^*_E} - \frac{1}{w'^*_E}\right) \; + \; \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \left(\frac{1}{w^*_E} - \frac{1}{w'^*_E}\right) \; + \\
& \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \left(\frac{1}{w^*_E} - \frac{1}{w'^*_E}\right)
\end{aligned}$$

$$\leq \quad 0 \tag{26}$$

$$\begin{aligned}
& \Delta t(T, R'_d, \mathcal{W}'^* \rightarrow \mathcal{W}^*) \\
= \;& R'_d \cdot c_0 \cdot \sum_{E \in T} (w'^*_E - w^*_E) \;+\; \mathcal{K}_2 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot (\frac{w'^*_{E'}}{w'^*_E} - \frac{w^*_{E'}}{w^*_E}) \;+ \\
& \mathcal{K}_3 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot (\frac{1}{w'^*_E} - \frac{1}{w^*_E}) \;+\; \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot (\frac{1}{w'^*_E} - \frac{1}{w^*_E}) \;+ \\
& \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot (\frac{1}{w'^*_E} - \frac{1}{w^*_E}) \\
\leq \;& 0
\end{aligned} \tag{27}$$

Summing up Eqn. (26) and Eqn. (27), we obtain

$$\Delta t(T, R_d, \mathcal{W}^* \rightarrow \mathcal{W}'^*) + \Delta t(T, R'_d, \mathcal{W}'^* \rightarrow \mathcal{W}^*) \;=\; c_0 \cdot (R_d - R'_d) \cdot \sum_{E \in T} (w^*_E - w'^*_E) \;\leq\; 0$$

Since $R_d < R'_d$, we have $\sum_{E \in T} (w^*_E - w'^*_E) \geq 0$, i.e. $area(\mathcal{W}^*) \geq area(\mathcal{W}'^*)$. □

Lemma 2 *Consider an edge E in the routing tree. Let w^*_E and w'^*_E be the width of the edge in assignments $\mathcal{W}^*$ and $\mathcal{W}'^*$ respectively. If $w^*_E < w'^*_E$, then*

$$\sum_{E' \in Ans(E)} H(E') \cdot (\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}) + \frac{H(E)}{w^*_E \cdot w'^*_E} \sum_{E' \in Des(E)} (w'^*_{E'} - w^*_{E'}) > 0 \tag{28}$$

Proof: Rewrite $t(T, R_d, \mathcal{W})$ in Eqn. (10) with respect to E as follows:

$$\begin{aligned}
t(T, R_d, \mathcal{W}) \;=\; & \mathcal{K}_0 \;+\; \left\{ R_d \cdot c_0 \cdot \sum_{E' \in T - \{E\}} w_{E'} \;+\; R_d \cdot c_0 \cdot w_E \right\} \;+ \\
& \left\{ \mathcal{K}_2 \cdot \sum_{E', E'' \in T - \{E\}, E' \neq E''} F(E', E'') \cdot \frac{w_{E''}}{w_{E'}} \;+\; \mathcal{K}_2 \cdot \sum_{E' \in Ans(E)} F(E', E) \cdot \frac{w_E}{w_{E'}} \;+ \right. \\
& \left. \mathcal{K}_2 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot \frac{w_{E'}}{w_E} \right\} \;+\; \left\{ \mathcal{K}_3 \cdot \sum_{E' \in T - \{E\}, E'' \in T, E' \neq E''} F(E', E'') \cdot \frac{1}{w_{E'}} \;+ \right. \\
& \left. \mathcal{K}_3 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot \frac{1}{w_E} \right\} \;+\; \left\{ \mathcal{K}_4 \cdot \sum_{E' \in T - \{E\}} G(E') \cdot \frac{1}{w_{E'}} \;+ \right. \\
& \left. \mathcal{K}_4 \cdot G(E) \cdot \frac{1}{w_E} \right\} \;+\; \left\{ \mathcal{K}_5 \cdot \sum_{E' \in T - \{E\}} H(E') \cdot \frac{1}{w_{E'}} \;+\; \mathcal{K}_5 \cdot H(E) \cdot \frac{1}{w_E} \right\}
\end{aligned} \tag{29}$$

Let $\mathcal{W}/E : w_E \rightarrow w'_E$ denote the wiresizing solution obtained by replacing w_E with w'_E in $\mathcal{W}$. The difference $\Delta t(T, R_d, \mathcal{W}^*/E : w^*_E \rightarrow w'^*_E)$, i.e. $t(T, R_d, \mathcal{W}^*) - t(T, R_d, \mathcal{W}^*/E : w^*_E \rightarrow w'^*_E)$, is given by:

$$\begin{aligned}
& \Delta t(T, R_d, \mathcal{W}^*/E : w^*_E \rightarrow w'^*_E) \\
= \;& R_d \cdot c_0 \cdot (w^*_E - w'^*_E) \;+\; \mathcal{K}_2 \cdot \sum_{E' \in Ans(E)} F(E', E) \cdot (\frac{w^*_E - w'^*_E}{w^*_{E'}}) \;+ \\
& \mathcal{K}_2 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot w^*_{E'} \cdot (\frac{1}{w^*_E} - \frac{1}{w'^*_E}) \;+\; \mathcal{K}_3 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot (\frac{1}{w^*_E} - \frac{1}{w'^*_E}) \;+
\end{aligned}$$

$$
\begin{aligned}
& \mathcal{K}_4 \cdot G(E) \cdot (\frac{1}{w_E^*} - \frac{1}{w_E'^*}) \ + \ \mathcal{K}_5 \cdot H(E) \cdot (\frac{1}{w_E^*} - \frac{1}{w_E'^*}) \\
\leq \ & 0
\end{aligned}
$$

Similarly, we can obtain $\Delta t(T, R_d', \mathcal{W}'^*/E : w_E'^* \to w_E^*)$ and deduce the following:

$$
\begin{aligned}
& \Delta t(T, R_d, \mathcal{W}^*/E : w_E^* \to w_E'^*) + \Delta t(T, R_d', \mathcal{W}'^*/E : w_E'^* \to w_E^*) \\
= \ & (R_d - R_d') \cdot c_0 \cdot (w_E^* - w_E'^*) \ + \ \mathcal{K}_2 \cdot \sum_{E' \in Ans(E)} F(E', E) \cdot (w_E^* - w_E'^*) \cdot (\frac{1}{w_{E'}^*} - \frac{1}{w_{E'}'^*}) \ + \\
& \mathcal{K}_2 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot (w_{E'}^* - w_{E'}'^*) \cdot (\frac{1}{w_E^*} - \frac{1}{w_E'^*}) \\
\leq \ & 0
\end{aligned}
$$

Since $w_E^* - w_E'^* < 0$ and $F(E_1, E_2) = H(E_1)$ if $E_2 \in Des(E_1)$,

$$
(R_d - R_d') \cdot c_0 \ + \ \mathcal{K}_2 \cdot \sum_{E' \in Ans(E)} H(E') \cdot (\frac{1}{w_{E'}^*} - \frac{1}{w_{E'}'^*}) \ + \ \mathcal{K}_2 \cdot \sum_{E' \in Des(E)} H(E) \cdot (w_{E'}'^* - w_{E'}^*) \cdot (\frac{1}{w_E^* \cdot w_E'^*}) \ \geq \ 0
$$

Since $R_d - R_d' < 0$ and $\mathcal{K}_2 > 0$, the result follows. □

As defined in [9, 10], a *single-stem tree* is a tree with only one segment (called the *stem segment* of that tree) incident on its root.

Lemma 3 *Consider a single stem tree T. Let E be the stem segment of tree T. If $R_d < R_d'$, then $w_E^* \geq w_E'^*$.*

Proof: Suppose $w_E^* < w_E'^*$, we obtain the following from Lemma 2:

$$
\frac{H(E)}{w_E^* \cdot w_E'^*} \cdot \sum_{E' \in Des(E)} (w_{E'}'^* - w_{E'}^*) \ > \ 0
$$

This implies that $\sum_{E' \in Des(E)} w_{E'}'^* > \sum_{E' \in Des(E)} w_{E'}^*$. Hence, $area(\mathcal{W}'^*) > area(\mathcal{W}^*)$. However, this contradicts Lemma 1. □

Lemma 4 *If $w_E^* < w_E'^*$ and $w_{E'}^* \geq w_{E'}'^*$ for all $E' \in Ans(E)$, then*

$$
\sum_{E' \in Des(E)} (w_{E'}'^* - w_{E'}^*) > 0 \tag{30}
$$

Proof: Since $\sum_{E' \in Ans(E)} H(E') \cdot (\frac{1}{w_{E'}^*} - \frac{1}{w_{E'}'^*}) \leq 0$, it follows directly from Lemma 2 that the following is true:

$$
H(E) \cdot \sum_{E' \in Des(E)} (w_{E'}'^* - w_{E'}^*) > 0
$$

Since $H(E) \geq 0$ (λ_i's are non-negative), it implies that $H(E) > 0$ and $\sum_{E' \in Des(E)} (w_{E'}'^* - w_{E'}^*) > 0$. □

Lemma 5 *If T is a single stem tree, then $R_d < R_d'$ implies $\mathcal{W}^*$ dominates $\mathcal{W}'^*$.*

Proof: Sort all edges in T according to a topological order starting from the stem. Let E be the first edge in this order such that $w_E^* < w_E'^*$. Then, for all $E' \in Ans(E)$, $w_{E'}^* \geq w_{E'}'^*$. We use P to denote the edges $E' \in Ans(E)$. By Lemma 3, P is not an empty set. Let T_E denote the sub-tree rooted at E (including E).

According to Theorem 2 (proof in Appendix), separability implies that the wire width assignment $\mathcal{W}^*$ on edge in T_E, denoted as $\mathcal{W}^*(T_E)$, is an optimal wire width assignment of T_E under the following objective (assuming that the wire widths of edges in P are fixed as specified by $\mathcal{W}^*$):

$$\begin{aligned}
t_P(T_E, R_d, \mathcal{W}^*) \;=\; & R_d \cdot c_0 \cdot \sum_{E' \in T_E} w^*_{E'} \;+\; \mathcal{K}_2 \cdot \sum_{E' \in P, E'' \in T_E} F(E', E'') \cdot \frac{w^*_{E''}}{w^*_{E'}} \;+ \\
& \mathcal{K}_2 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \frac{w^*_{E''}}{w^*_{E'}} \;+\; \mathcal{K}_3 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \frac{1}{w^*_{E'}} \;+ \\
& \mathcal{K}_4 \cdot \sum_{E' \in T_E} G(E') \cdot \frac{1}{w^*_{E'}} \;+\; \mathcal{K}_5 \cdot \sum_{E' \in T_E} H(E') \cdot \frac{1}{w^*_{E'}}
\end{aligned} \tag{31}$$

Let $\mathcal{W}^*/T_E : \mathcal{W}^* \to \mathcal{W}'^*$ denote the wire width assignment obtained by replacing the wire width assignment $\mathcal{W}^*(T_E)$ of T_E with $\mathcal{W}'^*(T_E)$, i.e. $(\mathcal{W}^* - \mathcal{W}^*(T_E)) \cup \mathcal{W}'^*(T_E)$. Similarly, let $\mathcal{W}'^*/T_E : \mathcal{W}'^* \to \mathcal{W}^*$ denote the wire width assignment obtained by replacing the wire width assignment $\mathcal{W}'^*(T_E)$ of T_E with $\mathcal{W}^*(T_E)$, i.e. $(\mathcal{W}'^* - \mathcal{W}'^*(T_E)) \cup \mathcal{W}^*(T_E)$. Comparing $t_P(T_E, R_d, \mathcal{W}^*)$ with $t_P(T_E, R_d, \mathcal{W}^*/T_E : \mathcal{W}^* \to \mathcal{W}'^*)$, we obtain the following inequality:

$$\begin{aligned}
& t_P(T_E, R_d, \mathcal{W}^*) - t_P(T_E, R_d, \mathcal{W}^*/T_E : \mathcal{W}^* \to \mathcal{W}'^*) \\
= \;& R_d \cdot c_0 \cdot \sum_{E' \in T_E} (w^*_{E'} - w'^*_{E'}) \;+\; \mathcal{K}_2 \cdot \sum_{E' \in P, E'' \in T_E} F(E', E'') \cdot \left(\frac{w^*_{E''}}{w^*_{E'}} - \frac{w'^*_{E''}}{w^*_{E'}}\right) \;+ \\
& \mathcal{K}_2 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \left(\frac{w^*_{E''}}{w^*_{E'}} - \frac{w'^*_{E''}}{w'^*_{E'}}\right) \;+\; \mathcal{K}_3 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \left(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}\right) \;+ \\
& \mathcal{K}_4 \cdot \sum_{E' \in T_E} G(E') \cdot \left(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}\right) \;+\; \mathcal{K}_5 \cdot \sum_{E' \in T_E} H(E') \cdot \left(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}\right) \\
\leq \;& 0
\end{aligned}$$

Similarly, comparing $t_P(T_E, R'_d, \mathcal{W}'^*)$ with $t_P(T_E, R'_d, \mathcal{W}'^*/T_E : \mathcal{W}'^* \to \mathcal{W}^*)$, we obtain the following inequality:

$$\begin{aligned}
& t_P(T_E, R'_d, \mathcal{W}'^*) - t_P(T_E, R'_d, \mathcal{W}'^*/T_E : \mathcal{W}'^* \to \mathcal{W}^*) \\
= \;& R'_d \cdot c_0 \cdot \sum_{E' \in T_E} (w'^*_{E'} - w^*_{E'}) \;+\; \mathcal{K}_2 \cdot \sum_{E' \in P, E'' \in T_E} F(E', E'') \cdot \left(\frac{w'^*_{E''}}{w'^*_{E'}} - \frac{w^*_{E''}}{w'^*_{E'}}\right) \;+ \\
& \mathcal{K}_2 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \left(\frac{w'^*_{E''}}{w'^*_{E'}} - \frac{w^*_{E''}}{w^*_{E'}}\right) \;+\; \mathcal{K}_3 \cdot \sum_{E', E'' \in T_E, E' \neq E''} F(E', E'') \cdot \left(\frac{1}{w'^*_{E'}} - \frac{1}{w^*_{E'}}\right) \;+ \\
& \mathcal{K}_4 \cdot \sum_{E' \in T_E} G(E') \cdot \left(\frac{1}{w'^*_{E'}} - \frac{1}{w^*_{E'}}\right) \;+\; \mathcal{K}_5 \cdot \sum_{E' \in T_E} H(E') \cdot \left(\frac{1}{w'^*_{E'}} - \frac{1}{w^*_{E'}}\right) \\
\leq \;& 0
\end{aligned}$$

Summing up the above two inequalities, we have:

$$(R_d - R'_d) \cdot c_0 \cdot \sum_{E' \in T_E} (w^*_{E'} - w'^*_{E'}) \;+\; \mathcal{K}_2 \cdot \sum_{E'' \in T_E} \left\{ (w^*_{E''} - w'^*_{E''}) \cdot \sum_{E' \in P} F(E', E'') \left(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}\right) \right\} \;\leq\; 0$$

Since $F(E', E'') = H(E')$ for $E' \in P$ and $E'' \in T_E$, we have:

$$(R_d - R'_d) \cdot c_0 \cdot \sum_{E' \in T_E} (w^*_{E'} - w'^*_{E'}) \;+\; \mathcal{K}_2 \cdot \sum_{E' \in P} H(E') \left(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}\right) \cdot \sum_{E'' \in T_E} w^*_{E''} - w'^*_{E''}) \;\leq\; 0$$

From Lemma 4, $\sum_{E' \in T_E}(w^*_{E'} - w'^*_{E'}) < 0$. In addition, we know that $R_d - R'_d < 0$ and $\mathcal{K}_2 > 0$. Therefore, we can deduce that

$$\sum_{E' \in P} H(E')(\frac{1}{w^*_{E'}} - \frac{1}{w'^*_{E'}}) \ > \ 0$$

This contradicts the assumption that $w^*_{E'} \geq w'^*_{E'}$ for all $E' \in P$. □

According to the separability, we can decompose T into several single-stem trees and optimize each single-stem tree independently. Applying Lemma 5 to each single-stem tree, we have:

Theorem 5 (DS/WS Relation): *For any tree T with one or more critical sinks, $R_d < R'_d$ implies $\mathcal{W}^*$ dominates $\mathcal{W}'^*$.* □

This result reveals the relation between driver sizing and wiresizing, and it plays an important role in determining the lower and upper bounds of the optimal k-SDWS-D solutions in next subsection.

3.2 Lower and Upper Bound Computation for Optimal k-SDWS-D Solutions

We first present an algorithm called the *k-SDWS/D LU-Bound* algorithm for computing the upper and lower bounds of an optimal k-SDWS-D solution for a given number of stage k: Starting with an initial wire width assignment (say, all segments have the minimum width), we compute the capacitive load of the routing tree. Based on Theorem 1, the optimal stage ratio, denoted by s, of the cascaded driver of k stage can be computed and a driver sizing solution is obtained. Now, we perform delay optimal wiresizing [10] on the routing tree T based on the resistance of the k-th driver. If the wire width assignment changes, the capacitive load changes. A new driver stage ratio is computed to yield a new optimal driver sizing solution. Then, the optimal wiresizing solution will be computed again based on the new driver size of the k-th driver. The process is repeated until the wire width assignment does not change in consecutive iterations. The algorithm is described formally in Table 1.

Let $\mathcal{W}_0$ be the initial minimum width assignment and $\mathcal{W}_i$ denote the optimal wire width assignment obtained in iteration i. Similarly, let R^i_d denote the resistance of the k-th driver at the beginning of iteration i. During iteration i ($i \geq 1$), R^i_d is computed based on the capacitive load $C_{IL}(T, \mathcal{W}_{i-1})$ and $\mathcal{W}_i$ is obtained based on R^i_d. It is obvious that in the first iteration, the wire widths in $\mathcal{W}_1$ is an upward revision of the wire width in $\mathcal{W}_0$ (since $\mathcal{W}_0$ is the minimum-width assignment). Hence, the capacitive load can only increases which implies an increase in the stage ratio and a decrease in the resistance of the k-th driver, i.e. $R^2_d < R^1_d$. According to Theorem 5, $\mathcal{W}_2$ dominates $\mathcal{W}_1$. In general, we can show by mathematical induction that $R^{i+1}_d \leq R^i_d$ (since $\mathcal{W}_i$ dominates $\mathcal{W}_{i-1}$) and in turn $\mathcal{W}_{i+1}$ dominates $\mathcal{W}_i$ (according to Theorem 5). Hence, the algorithm will terminate (since there is an upper bound on the maximum wire width) and indeed computes the lower bound of driver and wire sizes of the optimal k-SDWS-D solution. Similarly, we start with a maximum wire width assignment and compute the upper bound of driver and wire sizes of the optimal k-SDWS-D solution. Therefore, we have the following result:

Theorem 6 *Given a chain of k drivers, the k-SDWS/D LU-Bound algorithm computes the lower and upper bounds of an optimal k-SDWS-D solution.*

k-SDWS/D LU-Bound Algorithm

Function $\mathtt{k-SDWS/D\ LU-Bound}(T, R_{min}, k)$
/* Given a tree T, the minimum width transistor resistance R_{min}, and the stage number k, return the upper and lower bounds of the SDWS problem for delay minimization. */

$\mathcal{W}_l \leftarrow$ `Min_Wire_Width`;
while true
  Compute capacitive load: $C_{IL}(T, \mathcal{W}_l)$;
  Compute optimal driver stage ratio: $s_l \leftarrow (\frac{C_{IL}(T,\mathcal{W}_l)}{C_g})^{1/k}$;
  Compute the k-th driver resistance: $R_d \leftarrow \frac{R_{min}}{s_l^{(k-1)}}$;
  $\mathcal{W} \leftarrow$ `Delay_Optimal_Wiresizing`(R_d, T);
  if $\mathcal{W} > \mathcal{W}_l$ **then**
    $\mathcal{W}_l \leftarrow \mathcal{W}$
  else break;
end while
Output s_l as the stage ratio of the lower bound of driver sizing solution
  and $\mathcal{W}_l$ as the lower bound of wire sizing solution;
$\mathcal{W}_u \leftarrow$ `Max_Wire_Width`;
while true
  Compute capacitive load: $C_{IL}(T, \mathcal{W}_u)$;
  Compute optimal driver stage ratio: $s_u \leftarrow (\frac{C_{IL}(T,\mathcal{W}_u)}{C_g})^{1/k}$;
  Compute the k-th driver resistance: $R_d \leftarrow \frac{R_{min}}{s_u^{(k-1)}}$;
  $\mathcal{W} \leftarrow$ `Delay_Optimal_Wiresizing`(R_d, T);
  if $\mathcal{W} < \mathcal{W}_u$ **then**
    $\mathcal{W}_u \leftarrow \mathcal{W}$
  else break;
end while
Output s_u as the stage ratio of the upper bound of driver sizing solution
  and $\mathcal{W}_u$ as the upper bound of wire sizing solution;
end Function;

Table 1: The k-SDWS/D LU-Bound algorithm for computing lower and upper bounds of optimal SDWS solution for a given stage number k.

Proof: We give the proof for the lower bound computation only. The proof for upper bound can be derived similarly. Let $(\mathcal{D}^*, \mathcal{W}^*)$ be the optimal SDWS-D solution for a chain of k drivers and d_k^* be the optimal size of driver k. Let $(\mathcal{D}_i, \mathcal{W}_i)$ denote the driver and wiresizing solution computed in iteration i and d_k^i be the size of driver k in iteration i. We first show that $(\mathcal{D}_1, \mathcal{W}_1)$ is dominated by $(\mathcal{D}^*, \mathcal{W}^*)$.

Since $\mathcal{W}_0$ is dominated by $\mathcal{W}^*$, we have $C_{IL}(T, \mathcal{W}_0) \leq C_{IL}(T, \mathcal{W}^*)$. By Theorem 1,

$$d_k^1 \;=\; (\frac{C_{IL}(T, \mathcal{W}_0)}{C_g})^{(k-1)/k} \;\leq\; (\frac{C_{IL}(T, \mathcal{W}^*)}{C_g})^{(k-1)/k} \;=\; d_k^*$$

By Theorem 5, we conclude that $\mathcal{W}_1$ (which is computed based on R_d^1) is dominated by $\mathcal{W}^*$ since $R_d^1 = R_{min}/d_k^1 \geq R_{min}/d_k^* = R_d^*$ where R_d^* is the resistance of driver k in the optimal solution.

k-SDWS/D Optimal Algorithm

Function k − SDWS/D Optimal(T,R_{min}, k)
 /* Given a tree T, the minimum width transistor resistance R_{min}, and a stage number k, return the optimal stage ratio s, and the optimal wire width assignment $\mathcal{W}$. */

  Compute the upper and lower bounds: $\{s_u, s_l, \mathcal{W}_u, \mathcal{W}_l\} \leftarrow$ k − SDWS/D LU − Bound(T,R_{min}, k);
  if $\mathcal{W}_u > \mathcal{W}_l$ (upper and lower bounds do not meet) **then**
    Best_Delay $\leftarrow \infty$;
    Discretize possible driver sizes in the interval $[(s_l)^{k-1}, (s_u)^{k-1}]$;
    for each driver size d_p in $[(s_l)^{k-1}, (s_u)^{k-1}]$ **do**
      $d_k \leftarrow d_p$;
      Compute k-th driver resistance: $R_d \leftarrow \frac{R_{min}}{d_p}$
      $\mathcal{W} \leftarrow$ Delay_Optimal_Wiresizing(R_d, T);
      Compute driver sizes for $D_{1..k-1}$ according to Theorem 1;
      Current_Delay $\leftarrow t(T, k, \mathcal{D}, \mathcal{W})$;
      if Current_Delay < Best_Delay **then**
        Solution $\leftarrow \{\mathcal{D}, \mathcal{W}\}$;
        Best_Delay $\leftarrow$ Current_Delay;
    end for
  else /* $\mathcal{W}_u = \mathcal{W}_l$ and $s_u = s_l$ */
    Construct Solution from $\{s_u, s_l, \mathcal{W}_u, \mathcal{W}_l\}$;
    Best_Delay $\leftarrow t(T, k, \mathcal{D}, \mathcal{W})$;
  end if
  return Solution;
end Function;

Table 2: The k-SDWS/D Optimal algorithm for computing the optimal SDWS solution for a given stage number k.

SDWS/D-opt Algorithm

Function SDWS/D − opt(T,R_{min})
 /* Given a tree T, and the minimum width transistor resistance R_{min}, return the number of stages k, the stage ratio s, and the wire width assignment $\mathcal{W}$. */

  $k \leftarrow 1$;
  Best_Delay $\leftarrow \infty$;
  while true
    Compute optimal driver and wire sizing solution for k:
      $\{\mathcal{D}, \mathcal{W}\} \leftarrow$ k − SDWS/D Optimal(T,R_{min}, k);
    Current_Delay $\leftarrow t(T, k, \mathcal{D}, \mathcal{W})$;
    if Current_Delay < Best_Delay **then**
      Best_Solution $\leftarrow \{k, \mathcal{D}, \mathcal{W}\}$;
    else return Best_Solution;
    $k \leftarrow k + 1$;
  end while
end Function;

Table 3: The optimal SDWS/D-opt algorithm.

Assuming that $(\mathcal{D}_i, \mathcal{W}_i)$ is dominated by $(\mathcal{D}^*, \mathcal{W}^*)$, we can follow the same arguments and deduce that $(\mathcal{D}_{i+1}, \mathcal{W}_{i+1})$ is also dominated by $(\mathcal{D}^*, \mathcal{W}^*)$. Hence, the solution computed is a lower bound of the optimal solution for a given stage number k. $\square$

Experimental results show that the algorithm terminates after three or four iterations in most cases. In addition, the upper and lower bounds meet for most instances, which implies that the optimal k-SDWS-D solution is obtained. Note that the upper and lower bounds include both the driver and wire sizes.

3.3 Optimal Algorithm for the SDWS-D Problem

For a given stage number k, we compute the optimal driver and wire sizing solution as follows: we compute the upper and lower bounds of the k-SDWS-D optimal solutions using the k-SDWS/D LU-Bound algorithm. In the case where the bounds do not meet, we can obtain a set of discrete driver sizes defined by the bounds computed by the k-SDWS/D LU-Bound algorithm for the k-th driver. For each driver size, we can compute the optimal wiresizing solution using the algorithm in [10] and use Theorem 1 to compute the sizes of driver $D_2 \cdots D_{k-1}$ using $d_k \cdot C_g$ as the capacitive load that the $(k-1)$-stage drivers have to drive. The *k-SDWS/D Optimal* algorithm is given in Table 2.

Theorem 7 *Given a chain of k drivers and p possible sizes for the last driver and a routing tree with n segments and r possible wire widths, the worst case time complexity to compute the optimal driver and wire sizes for the k-SDWS-D problem is $O(p \cdot n^r)$.* $\square$

Note that p is usually very small since the lower and upper bounds computed in Section 3.2 are very tight (in fact, they meet for almost all test cases). The factor $O(n^r)$ is the worst case complexity of optimal wiresizing algorithm which in fact run in $O(n \cdot r)$ time based on effective lower and upper bound computation using the dominance property (Details of the optimal wiresizing algorithm can be found in [10]). Therefore, the k-SDWS/D Optimal algorithm runs in $O(n \cdot r)$ time in practice.

Our optimal *SDWS/D-opt* algorithm for SDWS-D problem performs a linear search for the number of stages k required, starting with $k = 1$. The process terminates when stage k do not perform better than stage $k-1$ (i.e. when adding an additional driver actually slows down the circuit). The algorithm is given in Table 3.

4 Simultaneous Driver and Wire Sizing for Both Delay and Power Optimization (SDWS-DP Problem)

In the SDWS-DP problem formulated in Section 2.2, the drivers and wires are sized to minimize the following objective function (Eqn. (20)):

$$obj(T, k, \mathcal{D}, \mathcal{W}) \;=\; \alpha \cdot Power(T, k, \mathcal{D}, \mathcal{W}) \;+\; \gamma \cdot t(T, k, \mathcal{D}, \mathcal{W})$$

We can adjust parameters α and γ to achieve smooth trade-off between performance and power. By choosing the parameters carefully, we can compute a driver and wire sizing solution to meet a delay constraint while minimizing the power dissipation.

In this section, we shall first study the properties of the optimal SDWS-DP solutions and then present an efficient algorithm for computing the optimal SDWS-DP solution.

4.1 Properties of Optimal SDWS Solutions for Both Delay and Power Optimization

The lemmas and theorems in this subsection are used to prove the correctness and optimality of the bound computation and optimal algorithm to the SDWS-DP problem. If the reader is only interested to learn the SDWS/DP algorithms, he/she may proceed directly to Section 4.2.

The following theorem defines a set of equations which will be used for optimal driver sizing solution computation for a fixed loading capacitance $C_{IL}(T, \mathcal{W})$ in Section 4.2.

Theorem 8 *Given a fixed loading capacitance $C_{IL}(T, \mathcal{W})$, the optimal driver size assignment $\mathcal{D}$ for a chain of k drivers satisfies the following equations when $\gamma > 0$:*

$$\begin{aligned} \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{1}{d_{i-1}} \ - \ \frac{d_{i+1}}{d_i^2} \right) &= 0 \textit{ for all } i = 2..k-1 \\ \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{1}{d_{k-1}} \ - \ \frac{C_{IL}(T, \mathcal{W})}{d_k^2 \cdot C_g} \right) &= 0 \end{aligned} \tag{32}$$

Proof: The optimal driver sizing solution minimizes the objective function specified by Eqn. (22):

$$obj_{T,k,\mathcal{W}}(\mathcal{D}) = \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{C_{IL}(T, \mathcal{W})}{d_k \cdot C_g} \ + \ \sum_{i=1}^{k-1} \frac{d_{i+1}}{d_i} \right)$$

Differentiating $obj_{T,k,\mathcal{W}}(\mathcal{D})$ with respect to d_i for $2 \le i \le k$, we obtain

$$\begin{aligned} \frac{\partial obj_{T,k,\mathcal{W}}(\mathcal{D})}{\partial d_i} &= \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{1}{d_{i-1}} \ - \ \frac{d_{i+1}}{d_i^2} \right) \text{ for all } i = 2..k-1 \\ \frac{\partial obj_{T,k,\mathcal{W}}(\mathcal{D})}{\partial d_k} &= \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \ + \ \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{1}{d_{k-1}} \ - \ \frac{C_{IL}(T, \mathcal{W})}{d_k^2 \cdot C_g} \right) \end{aligned}$$

By setting $\frac{\partial obj_{T,k,\mathcal{W}}(\mathcal{D})}{\partial d_i} = 0$ for $2 \le i \le k$, we obtain the system of equations given in Eqn. (32). □

We define the monotone and dominance properties for the driver sizing solutions.

Definition 4 *Given a chain of k cascaded drivers D_i's, a driver sizing solution $\mathcal{D}$ is a monotone assignment if $d_{i+1} > d_i$ for all $i = 1, 2, \cdots k-1$.*

Definition 5 *Given two driver sizing solutions $\mathcal{D} = \{d_1, d_2, \cdots, d_k\}$ and $\mathcal{D}' = \{d'_1, d'_2, \cdots, d'_k\}$, $\mathcal{D}$* dominates *$\mathcal{D}'$ if $d_i \ge d'_i$ for $1 \le i \le k$.*

Definition 6 *Given a chain of cascaded drivers D_i's and a driver size assignment $\mathcal{D}$ on D_i's, a* local refinement *on a driver D_i is the operation to optimize the size of D_i based on the objective function in Eqn. (22), without changing the sizes of other drivers specified by $\mathcal{D}$.*

In this paper, we have proved the following results:

Theorem 9 (Monotone Property): *For any given capacitive load $C_{IL}(T, \mathcal{W})$, any optimal driver sizing solution to the SDWS-DP problem under the combined delay and power optimization objective function specified by Eqn. (22) is monotone*[2].

Proof: Let $\mathcal{D}$ be the non-monotone optimal driver size assignment. Suppose j is the smallest index such that $d_j \leq d_{j-1}$ Let $\mathcal{D} - \{d_j\}$ be the assignment obtained after discarding driver D_j in the non-monotone optimal driver chain. For convenience, we use d_{k+1} to denote $\frac{C_{IL}(T,\mathcal{W})}{C_g}$. According to objective function defined in Eqn. (22), we have:

$$\begin{aligned} obj_{T,k,\mathcal{W}}(\mathcal{D}) &= \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} d_i \; + \; \gamma \cdot \mathcal{J}_2 \cdot \sum_{i=1}^{k} \frac{d_{i+1}}{d_i} \\ obj_{T,k-1,\mathcal{W}}(\mathcal{D} - \{d_i\}) &= \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2, i \neq j}^{k} d_i \; + \; \gamma \cdot \mathcal{J}_2 \cdot \left(\sum_{i=1}^{j-2} \frac{d_{i+1}}{d_i} \; + \; \frac{d_{j+1}}{d_{j-1}} \; + \; \sum_{i=j+1}^{k} \frac{d_{i+1}}{d_i} \right) \end{aligned}$$

Therefore,

$$\Delta \; = \; obj_{T,k,\mathcal{W}}(\mathcal{D}) \; - \; obj_{T,k-1,\mathcal{W}}(\mathcal{D} - \{d_i\}) \; = \; \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot d_j \; + \; \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{d_j}{d_{j-1}} + \frac{d_{j+1}}{d_j} - \frac{d_{j+1}}{d_{j-1}} \right)$$

Since $\frac{1}{d_j} - \frac{1}{d_{j-1}} \geq 0$, we have $\Delta > 0$, which contradicts the assumption that $\mathcal{D}$ is optimal. □

Theorem 10 (k-Monotone Property): *For a given capacitive load C_{IL} and a chain of $k \geq 2$ cascaded drivers D_i's,*

1. *if the condition*

$$\frac{C_{IL}}{C_g} \;\; > \;\; \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1 \right)^{2^{(k-1)}-1} \tag{33}$$

   holds, then there exists a monotone optimal driver size assignment $\mathcal{D}^*$ for the k-SDWS-DP problem under the objective function specified by Eqn. (22);

2. *if there exists a monotone optimal driver sizing solution for the k-SDWS-DP problem under the objective function specified by Eqn. (22), then*

$$\frac{C_{IL}}{C_g} \;\; > \;\; \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} \right)^{2^{(k-2)}-1} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1 \right)^{2^{(k-2)}} . \tag{34}$$

Proof: (Case 1) Solving Eqn. (32) for $k = 2$, we obtain:

$$d_2^2 \;\; = \;\; \left(\frac{C_{IL}}{C_g} \right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} \; + \; \frac{1}{d_1} \right)$$

Since $d_1 = 1$, the condition specified by Eqn. (33) holds implies that $d_2^2 > 1$. Hence, $d_2 > 1 = d_1$, which implies that the result is true for $k = 2$.

[2] In fact, this theorem and the following theorems in this section also hold for objective function specified by Eqn. (21).

Suppose the result is valid for $k = l$. Notice that $d_i \geq 1$ (Since minimum-size driver has size 1). Solving Eqn. (32) for $k = l+1$, we obtain:

$$\begin{aligned} d_{l+1}^2 &= \left(\frac{C_{IL}}{C_g}\right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + \frac{1}{d_l}\right) \\ &\geq \left(\frac{C_{IL}}{C_g}\right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right) \end{aligned}$$

Suppose condition specified by Eqn. (33) holds,

$$d_{l+1}^2 > \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^l - 2}$$

Taking square root,

$$d_{l+1} > \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^{(l-1)} - 1}$$

Since $d_{l+1} \cdot C_g$ is the capacitive load driven by the first l drivers and it satisfies condition (33) according to the inequality above. By the hypothesis, d_i's are monotone for $1 \leq i \leq l$. We only have to prove that $d_{l+1} > d_l$. According to Eqn. (32),

$$\begin{aligned} d_l^2 &= (d_{l-1} \cdot d_{l+1}) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot d_{l-1}}{\gamma \cdot \mathcal{J}_2} + 1\right) \\ &< d_{l-1} \cdot d_{l+1} \end{aligned}$$

Since $d_{l-1} < d_l$, we can conclude that $d_{l+1} > d_l$.

(Case 2) Solving Eqn. (32) for $k = 2$, we obtain:

$$d_2^2 = \left(\frac{C_{IL}}{C_g}\right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + \frac{1}{d_1}\right)$$

Since $d_1 = 1$, the existence of a monotone optimal solution implies that $d_2 > d_1 = 1$. Hence, we have $d_2^2 > 1$, which implies that the result is true for $k = 2$.

Suppose the result is true for $k = l$. Given a capacitive load C_{IL}, assume that we have a monotone optimal driver sizing solution for $k = l+1$. Since $d_{l+1} \cdot C_g$ is the capacitive load driven by the first l drivers, we have the following inequality (Eqn. (34)) by hypothesis:

$$d_{l+1} > \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2}\right)^{2^{(l-2)} - 1} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^{(l-2)}}$$

Solving Eqn. (32) for $k = l+1$, we obtain:

$$\begin{aligned} d_{l+1}^2 &= \left(\frac{C_{IL}}{C_g}\right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + \frac{1}{d_l}\right) \\ &> \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2}\right)^{2^{(l-1)} - 2} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^{(l-1)}} \end{aligned}$$

Solving for $\frac{C_{IL}}{C_g}$,

$$\begin{aligned} \frac{C_{IL}}{C_g} &> \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2}\right)^{2^{(l-1)} - 2} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^{(l-1)}} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + \frac{1}{d_l}\right) \\ &> \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2}\right)^{2^{(l-1)} - 1} \cdot \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2)}{\gamma \cdot \mathcal{J}_2} + 1\right)^{2^{(l-1)}} \end{aligned}$$

Hence, if there exists a monotone optimal driver sizing solution, the inequality in Eqn. (34) holds. □

Given a capacitive load C_{IL}, Theorem 10 allows us to determine, in most cases, the existence of a monotone driver sizing solution for a chain of k drivers quickly without solving the system of equations given in Eqn. (32). If the condition (33) is met, we can conclude that there exists a monotone optimal driver size assignment. On the other hand, if the inequality (34) does not hold, there is no monotone optimal driver sizing solution to the k-SDWS-DP problem. Otherwise, we have to solve the system of equations specified by Eqn. (32) to determine the existence of the monotone optimal driver sizing solution to the k-SDWS-DP problem.

Theorem 11 (Dominance Property): *Let $\mathcal{D}^*$ be an optimal driver size assignment. If a driver size assignment $\mathcal{D}$ dominates $\mathcal{D}^*$, then any local refinement of $\mathcal{D}$ still dominates $\mathcal{D}^*$. Similarly, if a driver size assignment $\mathcal{D}$ is dominated by $\mathcal{D}^*$, then any local refinement of $\mathcal{D}$ is dominated by $\mathcal{D}^*$.* □

Proof: Let $\mathcal{D} = \{d_1, d_2, \cdots, d_k\}$ and $\mathcal{D}^* = \{d_1^*, d_2^*, \cdots, d_k^*\}$. Let $\hat{d}_i$ be the size of driver D_i after local refinement operation on D_i with respect to driver size assignment $\mathcal{D}$. Denote the locally refined driver size assignment by $\mathcal{D}/D_i : d_i \rightarrow \hat{d}_i$. Similarly, let $\mathcal{D}/D_i : d_i \rightarrow d_i^*$ denote the assignment obtained by replacing d_i in $\mathcal{D}$ with d_i^*. For convenience, we use d_{k+1} to denote $\frac{C_{IL}(T,\mathcal{W})}{C_g}$. Then, we have:

$$
\begin{aligned}
& obj_{T,k,\mathcal{W}}(\mathcal{D}/D_i : d_i \rightarrow \hat{d}_i) \;-\; obj_{T,k,\mathcal{W}}(\mathcal{D}/D_i : d_i \rightarrow d_i^*) \\
= \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot (\hat{d}_i - d_i^*) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{\hat{d}_i}{d_{i-1}} - \frac{d_i^*}{d_{i-1}} + \frac{d_{i+1}}{\hat{d}_i} - \frac{d_{i+1}}{d_i^*} \right) \\
\leq \;& 0
\end{aligned} \tag{35}
$$

$$
\begin{aligned}
& obj_{T,k,\mathcal{W}}(\mathcal{D}^*) \;-\; obj_{T,k,\mathcal{W}}(\mathcal{D}^*/D_i : d_i^* \rightarrow \hat{d}_i) \\
= \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot (d_i^* - \hat{d}_i) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{d_i^*}{d_{i-1}^*} - \frac{\hat{d}_i}{d_{i-1}^*} + \frac{d_{i+1}^*}{d_i^*} - \frac{d_{i+1}^*}{\hat{d}_i} \right) \\
\leq \;& 0
\end{aligned} \tag{36}
$$

Summing up Eqn. (35) and Eqn. (36), we obtain:

$$
\begin{aligned}
& \frac{\hat{d}_i - d_i^*}{d_{i-1}} \;+\; d_{i+1} \cdot (\frac{1}{\hat{d}_i} - \frac{1}{d_i^*}) \;+\; \frac{d_i^* - \hat{d}_i}{d_{i-1}^*} \;+\; d_{i+1}^* \cdot (\frac{1}{d_i^*} - \frac{1}{\hat{d}_i}) \\
= \;& (\hat{d}_i - d_i^*) \cdot (\frac{1}{d_{i-1}} - \frac{1}{d_{i-1}^*}) \;+\; \frac{\hat{d}_i - d_i^*}{\hat{d}_i \cdot d_i^*} \cdot (d_{i+1}^* - d_{i+1}) \\
= \;& (\hat{d}_i - d_i^*) \cdot (\frac{d_{i-1}^* - d_{i-1}}{d_{i-1} \cdot d_{i-1}^*} + \frac{d_{i+1}^* - d_{i+1}}{\hat{d}_i \cdot d_i^*}) \\
\leq \;& 0
\end{aligned}
$$

If $\mathcal{D}^*$ is dominated by $\mathcal{D}$, which implies that the second product term has to be non-positive, then $\hat{d}_i - d_i^* \geq 0$. In other words, $\mathcal{D}/D_i : d_i \rightarrow \hat{d}_i$ still dominates $\mathcal{D}^*$. □

We shall show the following result which allows us to apply a similar approach as that in Section 3 to solve the SDWS-DP problem:

Theorem 12 (WS/DS Relation): *Given two wire width assignments $\mathcal{W}$ and $\mathcal{W}'$ for a routing tree T driven by a chain of k drivers. Let $\mathcal{D}$ and $\mathcal{D}'$ be the optimal driver sizing solutions for $\mathcal{W}$ and $\mathcal{W}'$, respectively. If $C_{IL}(T,\mathcal{W}) \geq C_{IL}(T,\mathcal{W}')$, then $\mathcal{D}$ dominates $\mathcal{D}'$.*

Proof: Let $\mathcal{D} = \{d_1, d_2, \cdots, d_k\}$ and $\mathcal{D}' = \{d'_1, d'_2, \cdots, d'_k\}$. First we show that $d_k \geq d'_k$.

$$\begin{aligned} & obj_{T,k,\mathcal{W}}(\mathcal{D}) - obj_{T,k,\mathcal{W}}(\mathcal{D}') \\ = \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} (d_i - d'_i) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{C_{IL}(T,\mathcal{W})}{C_g} \cdot (\frac{1}{d_k} - \frac{1}{d'_k}) \;+\; \sum_{i=1}^{k-1} (\frac{d_{i+1}}{d_i} - \frac{d'_{i+1}}{d'_i}) \right) \\ \leq \;& 0 \end{aligned} \tag{37}$$

$$\begin{aligned} & obj_{T,k,\mathcal{W}'}(\mathcal{D}') - obj_{T,k,\mathcal{W}'}(\mathcal{D}) \\ = \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{k} (d'_i - d_i) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left(\frac{C_{IL}(T,\mathcal{W}')}{C_g} \cdot (\frac{1}{d'_k} - \frac{1}{d_k}) \;+\; \sum_{i=1}^{k-1} (\frac{d'_{i+1}}{d'_i} - \frac{d_{i+1}}{d_i}) \right) \\ \leq \;& 0 \end{aligned} \tag{38}$$

Summing up Eqn. (37) and Eqn. (38), we obtain:

$$(C_{IL}(T,\mathcal{W}) - C_{IL}(T,\mathcal{W}')) \cdot (\frac{1}{d_k} - \frac{1}{d'_k}) \;\; \leq \;\; 0$$

Since $C_{IL}(T,\mathcal{W}) \geq C_{IL}(T,\mathcal{W}')$, we conclude that $d_k \geq d'_k$.

Given $1 < j \leq k$, suppose $d_i \geq d'_i$ for $j \leq i \leq k$. We want to show that $d_{j-1} \geq d'_{j-1}$ and hence prove the dominance relation by induction. Let $\mathcal{D}/d_{1..j-1} \rightarrow d'_{1..j-1}$ denote the driver size assignment by replacing the sizes of drivers $D_{1..j-1}$ in $\mathcal{D}$ by the corresponding sizes in $\mathcal{D}'$. Similarly, we define $\mathcal{D}'/d'_{1..j-1} \rightarrow d_{1..j-1}$ to be the driver size assignment by replacing the sizes of drivers $D_{1..j-1}$ in $\mathcal{D}'$ by the corresponding sizes in $\mathcal{D}$.

$$\begin{aligned} & obj_{T,k,\mathcal{W}}(\mathcal{D}) - obj_{T,k,\mathcal{W}}(\mathcal{D}/d_{1..j-1} \rightarrow d'_{1..j-1}) \\ = \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{j-1} (d_i - d'_i) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left\{ \sum_{i=1}^{j-2} \left(\frac{d_{i+1}}{d_i} - \frac{d'_{i+1}}{d'_i} \right) \;+\; \left(\frac{d_j}{d_{j-1}} - \frac{d_j}{d'_{j-1}} \right) \right\} \\ \leq \;& 0 \end{aligned}$$

$$\begin{aligned} & obj_{T,k,\mathcal{W}'}(\mathcal{D}') - obj_{T,k,\mathcal{W}'}(\mathcal{D}'/d'_{1..j-1} \rightarrow d_{1..j-1}) \\ = \;& \alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot \sum_{i=2}^{j-1} (d'_i - d_i) \;+\; \gamma \cdot \mathcal{J}_2 \cdot \left\{ \sum_{i=1}^{j-2} \left(\frac{d'_{i+1}}{d'_i} - \frac{d_{i+1}}{d_i} \right) \;+\; \left(\frac{d'_j}{d'_{j-1}} - \frac{d'_j}{d_{j-1}} \right) \right\} \\ \leq \;& 0 \end{aligned}$$

Summing up the above inequalities, we obtain:

$$(d_j - d'_j) \cdot (\frac{1}{d_{j-1}} - \frac{1}{d'_{j-1}}) \;\; \leq \;\; 0$$

Since $d_j - d'_j \geq 0$, we have $d_{i-1} \geq d'_{i-1}$. □

Lemma 6 *For a given capacitive load C_{IL} driven by a chain of $k \geq 2$ drivers, if there exists a monotone optimal k-SDWS-DP driver sizing solution, then there exists a monotone optimal k-SDWS-DP driver sizing solution for any capacitive load $C'_{IL} > C_{IL}$. Similarly, if there exists no monotone optimal k-stage driver sizing solution to the k-SDWS-DP problem for capacitive load C_{IL}, then there exists no monotone optimal k-SDWS-DP driver sizing solution for any capacitive load $C'_{IL} < C_{IL}$.*

Proof: It is trivially true for $k = 2$ (Theorem 10). Suppose this is true for $k = l$. Now, consider $k = l + 1$. Let d_{l+1} and d'_{l+1} be the optimal driver size for driver D_{l+1} driving C_{IL} and C'_{IL} respectively. According to Theorem 12, $d_{l+1} \leq d'_{l+1}$. By hypothesis, there exists a monotone optimal driver solution for a chain of l drivers driving a capacitive load of $d_{l+1} \cdot C_g$. We only have to show that $d'_{l+1} > d'_l$. By Eqn. (32),

$$\begin{aligned} d_l^2 &= (d_{l-1} \cdot d_{l+1}) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot d_{l-1}}{\gamma \cdot \mathcal{J}_2} + 1 \right) \\ &< d_{l-1} \cdot d_{l+1} \end{aligned}$$

Since $d_l > d_{l-1}$, we can conclude that $d_{l+1} > d_l$. Hence, there exists a monotone optimal driver sizing solution for a chain of k drivers. The other result follows directly. □

Theorem 13 *For a given capacitive load $C_{IL}(T, \mathcal{W})$, if there exists no monotone optimal driver sizing solution for a chain of k drivers, then there exists no monotone optimal driver sizing solution for a chain of $k+1$ drivers.*

Proof: Suppose there exists a monotone optimal driver sizing solution for a chain of $k + 1$ drivers. Let $\mathcal{D}$ and $\mathcal{D}'$ denotes the optimal driver sizing solution for the chain of k drivers and $k + 1$ drivers, respectively. Note that $\mathcal{D}$ is a non-monotone solution whereas $\mathcal{D}'$ is a monotone solution. First we show that $d'_{k+1} < \frac{C_{IL}(T,\mathcal{W})}{C_g}$. According to Eqn. (32),

$$\begin{aligned} d'^2_{k+1} &= \left(d'_k \cdot \frac{C_{IL}(T, \mathcal{W})}{C_g} \right) \Big/ \left(\frac{\alpha \cdot (\mathcal{L}_1 + \mathcal{L}_2) \cdot d'_k}{\gamma \cdot \mathcal{J}_2} + 1 \right) \\ &< d'_k \cdot \frac{C_{IL}(T, \mathcal{W})}{C_g} \end{aligned}$$

Since $d'_k < d'_{k+1}$, we conclude that $d'_{k+1} < \frac{C_{IL}(T,\mathcal{W})}{C_g}$. Since d'_i's for $1 \leq i \leq k + 1$ are monotone, there exists a monotone optimal solution for a chain of k drivers driving any capacitive load larger than $d'_{k+1} \cdot C_g$ (according to Lemma 6). However, this contradicts the assumption that there exists no monotone optimal solution for a chain of k drivers driving capacitive load $C_{IL}(T, \mathcal{W})$. □

Lemma 6 and Theorem 13 will be used in the next subsection to compute maximum possible number of drivers in an optimal SDWS-DP solution. Also, one can see that Formulation (24) implies that Theorems 2 through 5 in Sections 3.1.2 and 3.1.3 still apply to the optimal wiresizing solution under the combined delay and power optimization objective as defined in Eqn. (24). Therefore, the same optimal wiresizing solution algorithm in [10] can be used to optimize $obj_{T,k,\mathcal{D}}(\mathcal{W})$ in Eqn. (24).

4.2 Bound Computation and Optimal Algorithm for SDWS-DP Problem

For a given stage number k, we take the same approach as in solving the k-SDWS-D problem to compute the optimal solutions to the k-SDWS-DP problem: we first compute the upper and lower bounds of the optimal k-SDWS-DP solution. To compute the lower bound, we start with an initial wire width assignment in which all segments have minimum width wire. Based on the capacitive load of the routing tree, we compute a driver sizing solution using Eqn. (32). Then, the optimal wiresizing solution based on the current driver sizing solution is computed using the algorithm in [10]. The process of alternative driver sizing and wiresizing is repeated until the wire sizing solutions do not change in consecutive iterations. The upper bound is computed similarly by starting with maximum wire width assignment. The algorithm outlined above is referred to as the *k-SDWS/DP LU-Bound* algorithm (to differentiate it from the k-SDWS/D LU-Bound algorithm in which the driver sizing solution is computed differently). We have the following result (similar to the SDWS-D problem):

Theorem 14 *Given a chain of k drivers, the k-SDWS/DP LU-Bound algorithm computes the lower and upper bounds of an optimal k-SDWS-DP solution.*

Proof: We use the same notations introduced in the proof of Theorem 6. Again, we prove the lower bound case only. We first show that $(\mathcal{D}_1, \mathcal{W}_1)$ is dominated by $(\mathcal{D}^*, \mathcal{W}^*)$.

Since $\mathcal{W}_0$ is dominated by $\mathcal{W}^*$, we have $C_{IL}(T, \mathcal{W}_0) \leq C_{IL}(T, \mathcal{W}^*)$. By Theorem 12 (instead of Theorem 1), $\mathcal{D}_1$ is dominated by $\mathcal{D}^*$, which implies that $d_k^1 \leq d_k^*$. According to Theorem 5, $\mathcal{W}_1$ (computed based on R_d^1) is dominated by $\mathcal{W}^*$ since $R_d^1 = R_{min}/d_k^1 \geq R_{min}/d_k^* = R_d^*$, where R_d^* is the resistance of driver k in the optimal solution.

Assuming that $(\mathcal{D}_i, \mathcal{W}_i)$ is dominated by $(\mathcal{D}^*, \mathcal{W}^*)$, we can show similarly that $(\mathcal{D}_{i+1}, \mathcal{W}_{i+1})$ is also dominated by $(\mathcal{D}^*, \mathcal{W}^*)$. Hence, according to mathematical induction, the solution computed is a lower bound of the optimal solution for a given driver stage number k. □

Given the lower and upper bounds $[d_k^l, d_k^u]$ of the k-th driver, the *k-SDWS/DP Optimal* algorithm tries every possible driver size in $[d_k^l, d_k^u]$ for the k-th driver size. Again, Eqn. (32) (instead of Theorem 1) is used to compute the sizes of driver $D_2 \cdots D_{k-1}$ using $d_k \cdot C_g$ as the capacitive load that the $(k-1)$-stage drivers have to drive. For each possible d_k, the optimal wiresizing solution can still be computed using the algorithm in [10]. As in the SDWS-D problem, we have $d_k^l = d_k^u$ for most cases and a very small interval $[d_k^l, d_k^u]$ when $d_k^l \neq d_k^u$. We establish the following result which is similar to Theorem 7:

Theorem 15 *Given a chain of k drivers and p possible sizes for the last driver and a routing tree with n segments and r possible wire widths, let $T(k)$ be the time taken to compute the sizes of drivers $D_2 \cdots D_{k-1}$ given the sizes of D_k by solving the systems of equations in Eqn. (32). Then, the worst case time complexity to compute the optimal driver and wire sizes is $O(p \cdot (n^r + T(k)))$.* □

Again, the factor $O(n^r)$ is the worst case time complexity for computing an optimal wiresizing solution. In practice, when dominance property is used to compute the lower and upper bounds of the optimal wiresizing solution, this term is reduced to $O(r \cdot n)$ for almost all designs.

Due to the similarity between Eqn. (13) and Eqn. (24), optimal wiresizing solution under the combined objective of performance and power dissipation can be computed using the algorithm in [10]. However, computing an optimal driver sizing solution for a given capacitive load $C_{IL}(T, \mathcal{W})$ is more difficult. In the SDWS-D algorithms, the driver sizing solution is obtained according to Theorem 1 by computing a fixed stage ratio. In the SDWS-DP algorithms, we have to solve the set of equations specified in Eqn. (32). In our implementation, these equations are solved using MAPLE, a mathematical software for symbolic computation developed by University of Waterloo. Note that the dominance property is not used to compute the optimal driver sizing solution. We are currently looking into other approaches (for example, convex programming) in which the property can be useful.

To obtain the optimal stage number k^*_{DP}, the *SDWS/DP-opt* algorithm performs a search for $1 \leq k < k_{MAX}$ where k_{MAX} is the smallest stage number such that that capacitive load $C_{IL}(T, \mathcal{W}_{MAX})$ for a routing tree T with maximum wire width assignment $\mathcal{W}_{MAX}$ does not have a monotone optimal solution for a chain of k_{MAX} drivers.

Theorem 16 *Let k_{MAX} be the smallest stage number such that capacitive load $C_{IL}(T, \mathcal{W}_{MAX})$ for a routing tree T with maximum wire width assignment $\mathcal{W}_{MAX}$ does not have a monotone optimal solution for a chain of k_{MAX} drivers. There exists no monotone optimal driver sizing solution for any $k \geq k_{MAX}$ cascaded drivers given any wire width assignments.*

Proof: By Theorem 13, there exists no monotone optimal k-stage driver sizing solution for capacitive load $C_{IL}(T, \mathcal{W}_{MAX})$ for any $k \geq k_{MAX}$. Since $C_{IL}(T, \mathcal{W}_{MAX}) \geq C_{IL}(T, \mathcal{W})$ for any wire width assignment $\mathcal{W}$, we can conclude from Lemma 6 that there exists no monotone optimal k-stage driver sizing solution for $k \geq k_{MAX}$ given any wiresizing solution (including the optimal wiresizing solution). □

To compute k_{MAX}, we perform a linear search starting with $k = 1$. By Theorem 10, if the condition specified by Eqn. (33) is satisfied, there exist a monotone optimal solution for the k drivers. On the other hand, if the inequality specified by Eqn. (34) does not hold, there is no monotone optimal solution for the k drivers. Otherwise, the monotone property is verified by solving the system of equations given in Eqn. (32). We define k_{MAX} to be the first k such that the monotone property does not hold. By Theorem 13, there exists no monotone k-SDWS-DP optimal driver sizing solution for any $k > k_{MAX}$ cascaded drivers driving the capacitive load $C_{IL}(T, \mathcal{W}_{MAX})$.

Since all possible wire width assignments are dominated by $\mathcal{W}_{MAX}$, there exists no monotone optimal driver sizing solution for any $k \geq k_{MAX}$ cascaded drivers given any wire width assignments. Therefore, it is sufficient for the SDWS/DP-opt algorithm to compute, for each $1 \leq k < k_{MAX}$, the optimal wire and driver sizing solution (using the k-SDWS/DP Optimal algorithm). The best among the $k_{MAX} - 1$ solutions is the optimal SDWS-DP solution. The SDWS/DP-opt algorithm is given in Table 4.

5 Experimental Results

We have implemented the optimal SDWS/D and SDWS/DP algorithms in ANSI C for the Sun SPARC station environment. The algorithm is tested on a number of MCM and IC design examples consisting of a chain of cascaded drivers driving (1) a single sink net through a long interconnect and (2) a multiple-sink net through a tree-structure interconnect. HSPICE is used to simulate the circuit for accurate timing and power simulation

SDWS/DP-opt Algorithm
Function `SDWS/DP` $-$ `opt`$(T, R_{min}, \alpha, \gamma)$
/* Given a tree T, and the minimum width transistor resistance R_{min}, return the optimal number of stages k, the driver sizing solution $\mathcal{D}$, and the wire width assignment $\mathcal{W}$. */
if $\alpha = 0$ **then**
return `SDWS/D-opt`(T, R_{min}); /* Delay Optimization */
if $\gamma = 0$ **then**
return $k = 1$, $d_1 = 1$, $\mathcal{W} = \mathcal{W}_{MIN}$; /* Minimum Power Dissipation */
Compute k_{MAX};
`Best_Combined_Objective` $\leftarrow \infty$;
for $k = 1$ **to** $k_{MAX} - 1$ **do**
Compute optimal driver and wire sizing solution for k:
$\{\mathcal{D}, \mathcal{W}\} \leftarrow$ `k-SDWS/DP Optimal`(T, R_{min}, k);
`Current_Combined_Objective` $\leftarrow obj(T, k, \mathcal{D}, \mathcal{W})$;
if `Current_Combined_Objective` $<$ `Best_Combined_Objective` **then**
`Best_Solution` $\leftarrow \{k, \mathcal{D}, \mathcal{W}\}$;
end while
return `Best_Solution`;
end Function;

Table 4: The optimal SDWS/DP-opt algorithm.

Min Driver Resistance (Ω):	13598
Min Gate Capacitance (fF):	2.6802
Min Diffusion Capacitance (fF):	1.0403

Table 5: Technology parameters for CAZM $0.5\mu m$ CMOS drivers [14].

Parameters	MCM	IC
Min Loading Capacitance (fF):	1000	2.6802
Wire Resistance ($\Omega/\square$):	0.02	0.044
Wire Capacitance (area) ($aF/\mu m^2$):	3.46	41.3
Fringing Capacitance (2 sides) ($aF/\mu m$):	50.4	150

Table 6: Technology parameters based on (a) MCM10 technology [5] and (b) CAZM $0.5\mu m$ CMOS model [14].

to verify both our models and algorithms. The technology parameters used by HSPICE are summarized in Table 5 and 6.

The parameters for the driver are based on the CAZM $0.5\mu m$ CMOS process model [14]. The minimum driver resistance is obtained for a minimum size transistor (width = $1.0\mu m$, length = $0.5\mu m$) through HSPICE simulation of the drain-to-source current available when the drain-to-source voltage for a n-device is $0.95 \times V_{dd}$

($V_{dd} = 5.0V$). The minimum gate and diffusion capacitance is the gate and diffusion capacitance of a minimum size n-transistor. We assume in the experiments that drivers in all design examples (MCM and IC) are cascaded on-chip CMOS drivers. The minimum driver resistance, gate and diffusion capacitance are used to guide the design of drivers.

The minimum loading capacitance on a MCM substrate, which is the pad capacitance, is $1000fF$ whereas the minimum loading capacitance on an IC chip is the minimum gate capacitance. The interconnect parameters are obtained from MCM10 model [5] and CAZM $0.5\mu m$ CMOS process model [14].

5.1 Performance of SDWS/D Algorithm

In our experiments, we compare our SDWS/D wiresizing solutions with the solutions obtained using (a) driver sizing with constant stage ratio $s = e$ and minimum-wire-width (CDSMIN), (b) optimal driver sizing based on Theorem 1 and minimum-wire-width (ODSMIN), and (c) independent driver and wire sizing algorithm (DWSA), i.e. it performs driver sizing with constant stage ratio $s = e$ and optimal wiresizing [8]. The set of wire width allowed is $\{W_1, 2W_1, 3W_1, 4W_1\}$, where W_1 is the minimum width ($10\mu m$ in MCM10 technology and $0.95\mu m$ in IC technology). Hence, every wire segment in CDSMIN and ODSMIN has width W_1.

For the experiment on MCM design examples, we assume that the cascaded drivers are driving (a) a sink through a $5cm$ long interconnect, (b) a 4-sink net randomly placed on $10cm \times 10cm$ substrate, and (c) a 8-sink net randomly placed on $10cm \times 10cm$ substrate. In each case, the interconnect is divided into wire segments, each of length $100\mu m$ and modeled by a π-type RC circuit, in order to model the distributed nature of interconnect. For each test circuit in (b) and (c), we performed two sets of experiments. In the first set of experiments, we let the farthest sink from the source be the critical sink. In the second set of experiments, we randomly generate two critical sinks for 4-sink net and four critical sinks for 8-sinks net. The first driver in the chain is in turn driven by an ideal voltage source and the input signal is a square wave with rise and fall time of $1ns$ and a period of $40ns$ ($25MHz$).

Table 7 summarizes the signal delays by the four algorithms. In both sets of experiments, our SDWS/D algorithm consistently outperforms the other three methods. Compared with the traditional methods of constant-ratio driver sizing or optimal driver sizing with uniform wire width (CDSMIN and ODSMIN), our SDWS/D solutions achieved an improvement of up to 49% in both cases. Compared with the recently reported DWSA method [8], our SDWS/D algorithm can reduce the delay by up to 11%.

We perform the same set of experiments on the following IC design examples: (a) a sink through a $1cm$ long interconnect, (b) a 4-sink net randomly placed on $1cm \times 1cm$ IC chip, and (c) a 8-sink net randomly placed on $1cm \times 1cm$ IC chip. In the IC design, we segment the interconnect into grid edges of length $10\mu m$ and the sink capacitance is 10 times the minimum loading capacitance. The results are summarized in Table 8. Again, our SDWS/D algorithm consistently outperforms the other three methods. Compared with the CDSMIN, ODSMIN and DWSA methods, our SDWS/D solutions achieved an improvement of up to 49%, 47% and 12%, respectively.

Net	Single Critical Sink				Multiple Critical Sinks			
	CDSMIN	ODSMIN	DWSA	SDWS/D	CDSMIN	ODSMIN	DWSA	SDWS/D
1-sink	1.31	1.17	1.15	1.02	same as single critical sink			
4-sink	4.36	4.38	2.41	2.26	4.35	4.33	2.45	2.31
8-sink	5.54	5.53	2.82	2.80	4.05	3.63	2.24	2.14

Table 7: Average signal delay (ns) for (a) 1-critical-sink net and (b) multi-critical-sinks net under the MCM10 technology.

Net	Single Critical Sink				Multiple Critical Sinks			
	CDSMIN	ODSMIN	DWSA	SDWS/D	CDSMIN	ODSMIN	DWSA	SDWS/D
1-sink	1.54	1.48	1.05	0.95	same as single critical sink			
4-sink	2.21	2.13	1.35	1.19	2.14	2.05	1.28	1.17
8-sink	2.53	2.47	1.44	1.30	1.91	1.83	1.22	1.09

Table 8: Average signal delay (ns) for (a) 1-critical-sink net and (b) multi-critical-sinks net under the CAZM $0.5\mu m$ CMOS technology.

5.2 Performance of SDWS/DP Algorithm

We have studied the trade-off between power dissipation and delay using our SDWS/DP algorithm. For the same set of MCM 4-sink nets (with two critical sinks) in the previous experiment, we compute for each stage number $k = 2$ to 6, a driver and wire sizing solution optimizing the $obj(T, k, \mathcal{D}, \mathcal{W})$ for different α in Eqn. (25). Table 9 summarizes the results for a set of α parameters. For each α, the table lists the power dissipation (mW) and delay (ns) of the driver and wire sizing solution for each stage number $k = 2$ to 6. As one can see, by adjusting the value of α in objective function (25), one can achieve smooth trade-off between power dissipation and performance.

In Figure 4(a), the trade-off between delay and power dissipation for different k's is depicted by a set of curves. We can obtain a *contour* named *D/P-curve* which is dominated by the set of curves from above. Clearly, the D/P-curve represents best power and delay trade-off achieved by the optimal solutions of the SDWS/DP solutions. In Figure 4(b), we compare the solutions obtained by CDSMIN, ODSMIN and DWSA with the D/P-curve by the SDWS/DP algorithm. We can observe that the D/P-curve is dominated by the curves representing the solution sets by CDSMIN, ODSMIN and DWSA. One can always select a SDWS solution from the D/P-curve to meet a delay target with minimum power dissipation or to meet a power budget with best performance.

In Table 10, we compare the power requirement of the the test circuit under different design methods (CDSMIN, ODSMIN, DWSA and SDWS-DP) in order for the net to meet the delay specification. The table list a set of target delays that the net is expected to achieve and the most power economical solution by each design method under the performance requirement. An empty entry implies that the solution cannot meet

α	$k=2$		$k=3$		$k=4$		$k=5$		$k=6$	
	Power	Delay	Power	Delay	Power	Delay	Power	Delay	Power	Delay
0	31.42	9.075	81.08	3.787	128.5	2.785	174.9	2.488	211.0	2.411
0.1	28.89	9.076	69.56	3.863	100.3	2.808	109.2	2.525	113.2	2.417
0.2	28.07	9.077	51.66	4.156	74.31	3.010	95.02	2.648	97.09	2.545
0.3	27.79	9.121	47.90	4.448	65.18	3.212	76.79	2.772	78.14	2.761
0.4	27.02	9.352	43.43	4.750	58.11	3.444	65.87	3.148	66.92	3.186
0.5	26.00	9.756	39.49	5.298	50.71	3.870	59.70	3.278	59.32	3.449
0.6	25.03	10.085	36.30	5.751	45.25	4.439	51.19	3.852	51.39	3.938
0.7	23.29	10.929	33.44	6.407	40.09	5.100	45.39	4.256	45.82	4.498
0.8	20.22	13.178	29.08	7.724	36.70	5.478	39.81	5.190	40.05	5.218
0.9	16.64	16.696	25.63	9.103	33.63	6.244	33.63	6.505	34.74	6.601

Table 9: Power dissipation (mW) and delay (ns) for different α's under the MCM10 technology.

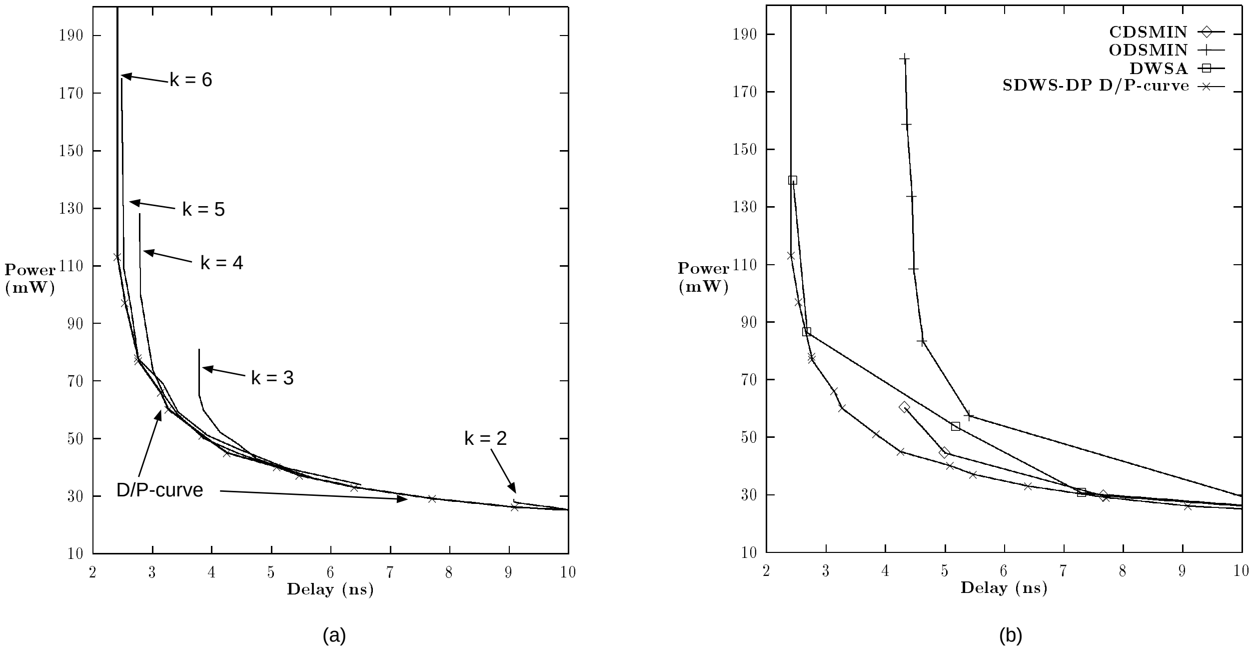

Figure 4: (a) D/P-curve containing the optimal SDWS/DP solutions (b) Comparisons between CDSMIN, ODSMIN, DWSA and SDWS/DP solutions under the MCM10 technology.

the delay specification. We can observe that our SDWS solutions require least power while meeting the delay specification. Our SDWS solutions achieved an reduction in power dissipation by up to 10%, 48% and 19% reduction, respectively, when compared with the CDSMIN, ODSMIN and DWSA methods. In addition, our SDWS solutions always require fewer stages of drivers (smaller k) which results in simpler layout design in

Delay	CDSMIN			ODSMIN			DWSA			SDWS-DP		
Constraint (ns)	Power	Delay	k	Power	Delay	k	Power	Delay	k	Power	Delay	k
10	29	7.67	5	29	10.00	2	30	7.31	5	26	9.10	3
5	44	4.99	7	83	4.63	4	54	3.86	6	43	4.74	3
4	-	-	-	-	-	-	54	3.86	6	50	3.87	4
3	-	-	-	-	-	-	86	2.69	7	77	2.77	5
2.5	-	-	-	-	-	-	139	2.45	8	113	2.41	6

Table 10: Comparisons of power requirement (mW) of various solutions meeting the delay specification (ns) for MCM design.

Delay	CDSMIN			ODSMIN			DWSA			SDWS-DP		
Constraint (ns)	Power	Delay	k	Power	Delay	k	Power	Delay	k	Power	Delay	k
5	7.7	3.69	4	8.3	4.11	2	8.0	3.66	4	6.6	4.47	2
4	7.7	3.69	4	15.0	2.48	3	8.0	3.66	4	7.0	4.00	3
3	11.9	2.31	5	15.0	2.48	3	13.8	1.87	5	8.8	2.76	3
2	-	-	-	32.3	2.05	6	13.8	1.87	5	11.8	2.00	4
1.5	-	-	-	-	-	-	23.2	1.37	6	16.8	1.47	4

Table 11: Comparisons of power requirement (mW) of various solutions meeting the delay specification (ns) for IC design.

practice.

We evaluate also the performance of our SDWS/DP algorithms on 4-sink nets (with two critical sinks) in IC routing used in the previous subsection. Table 11 compares the power requirement of the the test circuits under different design methods (CDSMIN, ODSMIN, DWSA and SDWS-DP) in order for the net to meet the delay specification. Our SDWS/DP algorithms can achieve up to 26%, 63% and 36% reduction in power as compared to the CDSMIN, ODSMIN and DWSA methods, respectively.

We can observe that by selecting α carefully, we can minimize power dissipation while meeting the delay constraint. This suggest an approach to solve the following optimization problem which was raised in [8]: Given a routing tree T and a performance specification B, determine the number of stages k, the set of driver sizes $\mathcal{D}$, and a wiresizing solution $\mathcal{W}$ on T, such that the performance measure $t(T,k,\mathcal{D},\mathcal{W})$ is bounded by B, i.e. $t(T,k,\mathcal{D},\mathcal{W}) \leq B$ and the power dissipation $Power(T,k,\mathcal{D},\mathcal{W})$ is minimized. We can solve the above problem by performing a binary search on α in Eqn. (25) where $0 \leq \alpha \leq 1$.

6 Conclusion and Future Work

To the best of our knowledge, this is the first paper which presents in-depth study of the simultaneous driver and wire sizing problem and its effect on performance and power optimization. The results in this paper have shown convincingly that simultaneous driver and wire sizing can lead to significant reduction in the interconnect delay and power dissipation. In high performance systems where the delays due to long on-chip interconnect and chip-to-chip interconnects are critical, our optimal solutions allow smaller driver size and/or fewer number of cascaded drivers required to drive long interconnect with proper wiresizing. As a result, our SDWS solutions provide a low power interconnect design for high performance circuits.

We would also like to generalize the driver sizing and wiresizing problem such that long interconnect lines can be segmented and interleaved with optimal size repeaters. Also, as mentioned in Section 1, interconnect topology optimization is another effective approach to reduce signal delay. A long term goal is to include wiresizing, driver sizing and also interconnect topology in the formulation of the power and performance optimization problem.

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Appendix

We shall prove the *Separability*, the *Monotone Property*, and the *Dominance Property*. In the following, we shall consider optimizing formulation (10) without constant term $\mathcal{K}_0$:

$$\begin{aligned} t(T, R_d, \mathcal{W}) \;\; = \;\; & \mathcal{K}_1 \cdot \sum_{E \in T} w_E \; + \; \mathcal{K}_2 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot \frac{w_{E'}}{w_E} \; + \\ & \mathcal{K}_3 \cdot \sum_{E, E' \in T, E \neq E'} F(E, E') \cdot \frac{1}{w_E} \; + \; \mathcal{K}_4 \cdot \sum_{E \in T} G(E) \cdot \frac{1}{w_E} \; + \\ & \mathcal{K}_5 \cdot \sum_{E \in T} H(E) \cdot \frac{1}{w_E} \end{aligned} \tag{39}$$

1 Separability

Proof: Let P be a path originated from the source, and $B = \{T_1, T_2, \cdots T_m\}$ be the set of subtrees branching off P. To simplify the notations, we define:

$$\begin{aligned} \mu(E, E') &= \mathcal{K}_2 \cdot F(E, E') \\ \omega(E, E') &= \mathcal{K}_3 \cdot F(E, E') \\ \nu(E) &= \mathcal{K}_4 \cdot G(E) \\ \phi(E) &= \mathcal{K}_5 \cdot H(E) \end{aligned}$$

We then rewrite Eqn. (39) as a function of the subtrees in B and the path P:

$$\begin{aligned} t(T, R_d, \mathcal{W}) \;\; = \;\; & \sum_{E \in T} \mathcal{K}_1 \cdot w_E \; + \sum_{E, E' \in T, E \neq E'} \mu(E, E') \cdot \frac{w_{E'}}{w_E} \; + \sum_{E, E' \in T, E \neq E'} \omega(E, E') \cdot \frac{1}{w_E} \; + \\ & \sum_{E \in T} \nu(E) \cdot \frac{1}{w_E} \; + \; \sum_{E \in T} \phi(E) \cdot \frac{1}{w_E} \\ = \;\; & \left[\sum_{b \in B} \left\{ \sum_{E \in b} \mathcal{K}_1 \cdot w_E \right\} \; + \; \sum_{E \in P} \mathcal{K}_1 \cdot w_E \right] \; + \; \left[\sum_{E, E' \in P, E \neq E'} \mu(E, E') \cdot \frac{w_{E'}}{w_E} \; + \right. \\ & \left. \sum_{b \in B} \left\{ \sum_{E \in P, E' \in b} \mu(E, E') \cdot \frac{w_{E'}}{w_E} \right\} \; + \; \sum_{b \in B} \left\{ \sum_{E, E' \in b, E \neq E'} \mu(E, E') \cdot \frac{w_{E'}}{w_E} \right\} \right] \; + \\ & \left[\sum_{E, E' \in P, E \neq E'} \omega(E, E') \cdot \frac{1}{w_E} \; + \; \sum_{b \in B} \left\{ \sum_{E \in P, E' \in b} \omega(E, E') \cdot \frac{1}{w_E} \right\} \right. . \; + \\ & \left. \sum_{b \in B} \left\{ \sum_{E, E' \in b, E \neq E'} \omega(E, E') \cdot \frac{1}{w_E} \right\} \right] \; + \; \left[\sum_{E \in P} \nu(E) \cdot \frac{1}{w_E} \; + \; \sum_{b \in B} \left\{ \sum_{E \in b} \nu(E) \cdot \frac{1}{w_E} \right\} \right] \; + \\ & \left[\sum_{E \in P} \phi(E) \cdot \frac{1}{w_E} \; + \; \sum_{b \in B} \left\{ \sum_{E \in b} \phi(E) \cdot \frac{1}{w_E} \right\} \right] \end{aligned}$$

We define:

$$t_{P,1} \;\; = \;\; \sum_{E \in P} \mathcal{K}_1 \cdot w_E \; + \sum_{E, E' \in P, E \neq E'} \mu(E, E') \cdot \frac{w_{E'}}{w_E} \; + \sum_{E, E' \in P, E \neq E'} \omega(E, E') \cdot \frac{1}{w_E} \; +$$

$$\sum_{b \in B} \left\{ \sum_{E \in P, E' \in b} \omega(E,E') \cdot \frac{1}{w_E} \right\} + \sum_{E \in P} \nu(E) \cdot \frac{1}{w_E} + \sum_{E \in P} \phi(E) \cdot \frac{1}{w_E} \tag{40}$$

$$\begin{aligned} t_{P,2}(b) &= \sum_{E \in b} \mathcal{K}_1 \cdot w_E + \sum_{E \in P, E' \in b} \mu(E,E') \cdot \frac{w_{E'}}{w_E} + \sum_{E,E' \in b, E \neq E'} \mu(E,E') \cdot \frac{w_{E'}}{w_E} + \\ & \sum_{E,E' \in b, E \neq E'} \omega(E,E') \cdot \frac{1}{w_E} + \sum_{E \in b} \nu(E) \cdot \frac{1}{w_E} + \sum_{E \in b} \phi(E) \cdot \frac{1}{w_E} \end{aligned} \tag{41}$$

We then have:

$$t(T, R_d, \mathcal{W}) = t_{P,1} + \sum_{b \in B} t_{P,2}(b) \tag{42}$$

where $t_{P,1}$ is a constant because it depends only on the width assignment of the path P. For any $b \in B$, $t_{P,2}(b)$ is a function whose only variables are the widths of the segments in the subtree b (assuming that the segment widths in P are given). Since the contribution from each subtree b to the summation is independent of each other, $t(T, R_d, \mathcal{W})$ is optimized if and only if for each $b \in B$, $t_{P,2}(b)$ is optimized. Separability follows as a consequence. □

2 Monotone Property

Proof: Assume that the monotone property fails for a tree T, that is, all the optimal width assignments are not monotone. Then for any optimal assignment $\mathcal{W}^*$, there must exist two adjacent edges E_1 and E_2 such that $E_1 \in Ans(E_2)$, and $w_{E_1} < w_{E_2}$. Since $\mathcal{W}^*$ is optimal, there is a non-negative increase in the cost function when we change the width of E_2 in $\mathcal{W}^*$ from w_{E_2} to w_{E_1}:

$$\begin{aligned} & \Delta t(T, R_d, \mathcal{W}^*/E_2 : w_{E_2} \to w_{E_1}) \\ = \;& t(T, R_d, \mathcal{W}^*) - t(T, R_d, \mathcal{W}^*/E_2 : w_{E_2} \to w_{E_1}) \\ = \;& \mathcal{K}_1 \cdot (w_{E_2} - w_{E_1}) + \mathcal{K}_2 \cdot \sum_{E' \in Ans(E_2)} \cdot F(E', E_2) \cdot \frac{w_{E_2} - w_{E_1}}{w_{E'}} + \\ & \mathcal{K}_2 \cdot \sum_{E' \in Des(E_2)} F(E_2, E') \cdot (\frac{w_{E'}}{w_{E_2}} - \frac{w_{E'}}{w_{E_1}}) + \mathcal{K}_3 \cdot \sum_{E' \in Des(E_2)} F(E_2, E') \cdot (\frac{1}{w_{E_2}} - \frac{1}{w_{E_1}}) + \\ & \mathcal{K}_4 \cdot G(E_2) \cdot (\frac{1}{w_{E_2}} - \frac{1}{w_{E_1}}) + \mathcal{K}_5 \cdot H(E_2) \cdot (\frac{1}{w_{E_2}} - \frac{1}{w_{E_1}}) \\ \leq \;& 0 \end{aligned}$$

Moreover, there is a non-negative increase in the cost function when we change the width of E_1 from w_{E_1} to w_{E_2}:

$$\begin{aligned} & \Delta t(T, R_d, \mathcal{W}^*/E_1 : w_{E_1} \to w_{E_2}) \\ = \;& t(T, R_d, \mathcal{W}^*) - t(T, R_d, \mathcal{W}^*/E_1 : w_{E_1} \to w_{E_2}) \\ = \;& \mathcal{K}_1 \cdot (w_{E_1} - w_{E_2}) + \mathcal{K}_2 \cdot \sum_{E' \in Ans(E_1)} F(E', E_1) \cdot \frac{w_{E_1} - w_{E_2}}{w_{E'}} + \\ & \mathcal{K}_2 \cdot \sum_{E' \in Des(E_1)} F(E_1, E') \cdot (\frac{w_{E'}}{w_{E_1}} - \frac{w_{E'}}{w_{E_2}}) + \mathcal{K}_3 \cdot \sum_{E' \in Des(E_1)} F(E_1, E') \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) + \end{aligned}$$

$$
\begin{aligned}
& \mathcal{K}_4 \cdot G(E_1) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \ + \ \mathcal{K}_5 \cdot H(E_1) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \\
\leq \ & 0
\end{aligned}
$$

If we compare $-\Delta t(T, R_d, \mathcal{W}^*/E_2 : w_{E_2} \rightarrow w_{E_1})$ with $\Delta t(T, R_d, \mathcal{W}^*/E_1 : w_{E_1} \rightarrow w_{E_2})$ term-by-term and use the properties of the F, G and H functions in (12), we have:

$$
\mathcal{K}_1 \cdot (w_{E_1} - w_{E_2}) \ = \ \mathcal{K}_1 \cdot (w_{E_1} - w_{E_2}) \tag{43}
$$

$$
\mathcal{K}_2 \cdot \sum_{E' \in Ans(E_2)} F(E', E_2) \cdot \frac{w_{E_1} - w_{E_2}}{w_{E'}} \ \leq \ \mathcal{K}_2 \cdot \sum_{E' \in Ans(E_1)} F(E', E_1) \cdot \frac{w_{E_1} - w_{E_2}}{w_{E'}} \tag{44}
$$

$$
\mathcal{K}_2 \cdot \sum_{E' \in Des(E_2)} F(E_2, E') \cdot (\frac{w_{E'}}{w_{E_1}} - \frac{w_{E'}}{w_{E_2}}) \ \leq \ \mathcal{K}_2 \cdot \sum_{E' \in Des(E_1)} F(E_1, E') \cdot (\frac{w_{E'}}{w_{E_1}} - \frac{w_{E'}}{w_{E_2}}) \tag{45}
$$

$$
\mathcal{K}_3 \cdot \sum_{E' \in Des(E_2)} F(E_2, E') \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \ \leq \ \mathcal{K}_3 \cdot \sum_{E' \in Des(E_1)} F(E_1, E') \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \tag{46}
$$

$$
\mathcal{K}_4 \cdot G(E_2) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \ \leq \ \mathcal{K}_4 \cdot G(E_1) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \tag{47}
$$

$$
\mathcal{K}_5 \cdot H(E_2) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \ \leq \ \mathcal{K}_5 \cdot H(E_1) \cdot (\frac{1}{w_{E_1}} - \frac{1}{w_{E_2}}) \tag{48}
$$

Summing up the inequalities (43)–(48), we have:

$$
\Delta t(T, R_d, \mathcal{W}^*/E_1 : w_{E_1} \rightarrow w_{E_2}) \ \geq \ -\Delta t(T, R_d, \mathcal{W}^*/E_2 : w_{E_2} \rightarrow w_{E_1}) \ \geq \ 0
$$

Therefore, we can elminate the non-monotonicity between E_1 and E_2 by changing the width of E_1 from w_{E_1} to w_{E_2} without increasing the cost function. In other words, we can transform a non-monotone optimal assignment to a monotone assignment without increasing the cost function. □

3 Dominance Property

Proof: Define

$$
\begin{aligned}
\Psi(\mathcal{W}, \overline{E}) \ = \ & \mathcal{K}_1 \cdot \sum_{E' \in T - \{E\}} w_{E'} \ + \ \mathcal{K}_2 \cdot \sum_{E', E'' \in T - \{E\}, E' \neq E''} F(E', E'') \cdot \frac{w_{E''}}{w_{E'}} \ + \\
& \mathcal{K}_3 \cdot \sum_{E', E'' \in T - \{E\}, E' \neq E''} F(E', E'') \cdot \frac{1}{w_{E'}} \ + \ \mathcal{K}_3 \cdot \sum_{E' \in Ans(E)} F(E', E) \cdot \frac{1}{w_{E'}} \ + \\
& \mathcal{K}_4 \cdot \sum_{E' \in T - \{E\}} G(E') \cdot \frac{1}{w_{E'}} \ + \ \mathcal{K}_5 \cdot \sum_{E' \in T - \{E\}} H(E') \cdot \frac{1}{w_{E'}} \\
\Phi(\mathcal{W}, \overline{E}) \ = \ & \mathcal{K}_1 \ + \ \mathcal{K}_2 \cdot \sum_{E' \in Ans(E)} F(E', E) \cdot \frac{1}{w_{E'}} \\
\Theta(\mathcal{W}, \overline{E}) \ = \ & \mathcal{K}_2 \cdot \sum_{E' \in Des(E)} F(E, E') \cdot w_{E'} \ + \ \mathcal{K}_3 \cdot \sum_{E' \in Des(E)} F(E, E') \ + \ \mathcal{K}_4 \cdot G(E) \ + \ \mathcal{K}_5 \cdot H(E)
\end{aligned}
$$

We can then rewrite (39) as follows:

$$
t(T, R_d, \mathcal{W}) \ = \ \Psi(\mathcal{W}, \overline{E}) \ + \ \Phi(\mathcal{W}, \overline{E}) \cdot w_E \ + \ \Theta(\mathcal{W}, \overline{E}) \cdot \frac{1}{w_E} \tag{49}
$$

Since $\Psi(\mathcal{W}, \overline{E})$, $\Phi(\mathcal{W}, \overline{E})$, and $\Theta(\mathcal{W}, \overline{E})$ are independent of w_E, they are considered as constant for local refinement of E. Minimizing (49) gives the local refinement $\tilde{w_E}$ of segment E. Notice that for any pair of wiresizing solutions $\mathcal{W}$ and $\mathcal{W}'$ such that $\mathcal{W}'$ dominates $\mathcal{W}$. We have $\Phi(\mathcal{W},\overline{E}) \geq \Phi(\mathcal{W}',\overline{E})$ and $\Theta(\mathcal{W},\overline{E}) \leq \Theta(\mathcal{W}',\overline{E})$.

Let w_E^* be the width for segment E in the optimal assignment $\mathcal{W}^*$. We have:

$$\Psi(\mathcal{W},\overline{E}) \;+\; \Phi(\mathcal{W},\overline{E})\cdot \tilde{w_E} \;+\; \Theta(\mathcal{W},\overline{E})\cdot\frac{1}{\tilde{w_E}} \;\leq\; \Psi(\mathcal{W},\overline{E}) \;+\; \Phi(\mathcal{W},\overline{E})\cdot w_E^* \;+\; \Theta(\mathcal{W},\overline{E})\cdot\frac{1}{w_E^*} \tag{50}$$

Since w_E^* is also the *locally* optimal width assignment for edge E with respect to the rest of the width assignment in $\mathcal{W}^*$, we have:

$$\Psi(\mathcal{W}^*,\overline{E}) \;+\; \Phi(\mathcal{W}^*,\overline{E})\cdot w_E^* \;+\; \Theta(\mathcal{W}^*,\overline{E})\cdot\frac{1}{w_E^*} \;\leq\; \Psi(\mathcal{W}^*,\overline{E}) \;+\; \Phi(\mathcal{W}^*,\overline{E})\cdot \tilde{w_E} \;+\; \Theta(\mathcal{W}^*,\overline{E})\cdot\frac{1}{\tilde{w_E}} \tag{51}$$

Summing up (50) and (51), we obtain:

$$\begin{aligned} \left\{\Phi(\mathcal{W},\overline{E})-\Phi(\mathcal{W}^*,\overline{E})\right\}\cdot\{\tilde{w_E}-w_E^*\} \;+\; \left\{\Theta(\mathcal{W},\overline{E})-\Theta(\mathcal{W}^*,\overline{E})\right\}\cdot\left\{\frac{1}{\tilde{w_E}}-\frac{1}{w_E^*}\right\} &\;\leq\; 0 \\ \Rightarrow \left\{\Phi(\mathcal{W},\overline{E})-\Phi(\mathcal{W}^*,\overline{E}) \;+\; \frac{\Theta(\mathcal{W}^*,\overline{E})-\Theta(\mathcal{W},\overline{E})}{\tilde{w_E}\cdot w_E^*}\right\}\cdot\{\tilde{w_E}-w_E^*\} &\;\leq\; 0 \end{aligned}$$

If $\mathcal{W}$ dominates $\mathcal{W}^*$, we have $\Phi(\mathcal{W},\overline{E}) \leq \Phi(\mathcal{W}^*,\overline{E})$ and $\Theta(\mathcal{W}^*,\overline{E}) \leq \Theta(\mathcal{W},\overline{E})$, and therefore $\tilde{w_E} - w_E^* \geq 0$ (i.e. the refinement of $\mathcal{W}$ still dominates $\mathcal{W}^*$). Similarly, if $\mathcal{W}^*$ dominates $\mathcal{W}$, then $\mathcal{W}^*$ dominates the local refinement of $\mathcal{W}$. $\square$