ABSTRACT OF THE DISSERTATION

Crossbar Arbitration in Interconnection Networks
for Multiprocessors and Multicomputers

by

Hsin-Chou Chi
University of California, Los Angeles, 1994
Professor Yuval Tamir, Chair

Small crossbars are key components of communication switches used in interconnection networks for multiprocessors and multicomputers. The traffic through the switches is often delayed due to conflicting demands for resources, such as buffer space or output ports. Hence, switches must include *arbiters* that resolve conflicting resource demands. Efficient design and implementation of these arbiters is critical for maximizing network performance.

In order to maximize performance, recent communication switch designs allow packets at an input port, destined to different output ports, to be transmitted through the switch in any order. In this dissertation several *symmetric crossbar arbiters* which can be used in this type of switches are proposed. These arbiter designs are compared based on simulations of a multistage interconnection network, VLSI implementation, and circuit simulation. Two efficient arbiter implementations are described.

For a fixed number of nodes, larger crossbars result in reduced probability of conflicts and allows packets to traverse the network in fewer hops. However, the increased arbitration delay can lead to overall poor network performance. A technique is proposed for the arbiter design in asynchronous networks, which can

mitigate the impact of the increased arbitration delay by decomposing the arbitration process into multiple steps.

While our symmetric crossbar arbiters lead to excellent performance in terms of throughput and average latency, they do not guarantee *fairness*. Hence, it is possible for an ‘‘unlucky’’ packet to be left in a switch buffer for a long time, potentially forever, while other packets are forwarded quickly through the switch. We introduce and evaluate a technique for preventing such *starvation* situations.

Finally, we describe how our proposed arbiters can be used to support adaptive routing and high-priority traffic in interconnection networks. Efficient arbiter designs for these two applications are described.