# Analytical Delay Models for VLSI Interconnects Under Ramp Input

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## Abstract

For typical $RLC$ interconnections with ramp input as the source voltage, Elmore delay can deviate significantly (by up to 100% or more) from SPICE-computed delay since it is independent of rise time of the input ramp signal. However, Elmore delay has been widely used as an analytical estimate of interconnect delays in the performance-driven synthesis and layout of VLSI routing topologies. Here, we develop new analytical delay models based on the first and second moments of the interconnect transfer function when the input is a ramp signal with finite rise time. Delay estimates using our first moment based analytical models are within 4% of SPICE-computed delay, and models based on both first and second moments are within 2.3% of SPICE, across a wide range of interconnect parameter values. Our analytical models are several several orders of magnitude faster to evaluate than simulation methodologies such as SPICE. We also describe extensions of our approach for estimation of source-sink delays in arbitrary interconnect trees.

## 1 Introduction

Accurate calculation of propagation delay in VLSI interconnects is critical to the design of high speed systems, and transmission line effects now play an important role in determining interconnect delays and system performance. Existing techniques are based on either *simulation* or (closed-form) *analytical formulas*. Simulation methods such as SPICE give the most accurate insight into arbitrary interconnect structures, but are computationally expensive. Faster methods based on moment matching techniques are proposed in [10, 12, 11, 14], but are still too expensive to be used during layout optimization. Thus, Elmore delay [2], a first order approximation of

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delay under step input, is still the most widely used delay model in the performance-driven routing of clock distribution and Steiner global routing topologies. However, Elmore delay cannot be applied to estimate the delay for interconnect lines with ramp input source; this inaccuracy is harmful to current performance-driven routing methods which try to determine optimal interconnect segment lengths and widths (as well as driver sizes). Recently, [4] has claimed that Elmore delay is an upper bound on the 50% threshold delay for $RC$ interconnection trees, for any general input waveform.[1] However, we find that Elmore delay is not at all close to SPICE-computed 50% threshold delays and can deviate as much as 100% from the SPICE-computed delays (see Section 7 below).

Previous moment-based approaches [10, 12, 14] can compute a response for interconnects under ramp input within a simulation-based methodology, but no previous work has given any *analytical* delay estimation model based on the first few moments. This paper gives a new and accurate *analytical* delay estimate for distributed $RLC$ interconnects under ramp input. To experimentally validate our analysis and delay formula, we model VLSI interconnect lines having various combinations of source, load parameters and different input rise times, and obtain delay estimates from SPICE, Elmore delay and the proposed analytical delay model. Over our range of test cases, Elmore delay estimates can be as much as 100% away from the SPICE-computed delays. As the rise time of the input signal increases, Elmore delay deviates even further from SPICE-computed delays, which is unacceptable for design applications. In contrast, our single-pole delay estimates are within 4% of SPICE delays and our two-pole delay estimates are within 2.3% of SPICE delays. Since our analytical models have the same time complexity of evaluation as the Elmore model, we believe that they are very useful for performance-driven routing methodologies.

The organization of our paper is as follows. In Section 2 we discuss delay models which have been previously proposed for interconnect lines under step input. Section 3 presents a new analytical delay definition for interconnect lines under ramp input. Section 4 discusses various threshold delay models for single-pole approximation of the interconnect transfer function; Section 5 gives various threshold delay models for two-pole approximation; and Section 6 extends our

[1] Our convention is to define threshold threshold delays relative to the point where the input signal is zero. However, the sense of [4] is that threshold delay means "threshold to threshold" delay: measure from when the input crosses a given threshold to when the output crosses the same threshold. E.g., in our convention 50% Elmore delay for ramp input becomes $\frac{T_R}{2} + b_1$ instead of just $b_1$ as in [4].

delay modeling approach to interconnection trees. Section 7 concludes with experimental results for various combinations of input rise times and interconnect parameters.

## 2 Previous Delay Models Under Step Input

The transfer function of an $RLC$ interconnect line with source and load impedance (Figure 1) can be obtained using the ABCD parameters [1] as

$$\begin{aligned} H(s) &= \frac{V_2(s)}{V_0(s)} = \frac{1}{\left[\cosh(\theta h) + \frac{Z_S}{Z_0}\sinh(\theta h)\right] + \frac{1}{Z_T}\left[Z_0\sinh(\theta h) + Z_S\cosh(\theta h)\right]} \\ &= \frac{1}{1 + b_1 s + b_2 s^2 + \ldots + b_k s^k + \ldots} \end{aligned} \quad (1)$$

where $\theta = \sqrt{(r+sl)sc}$ is the propagation constant and $Z_0 = \sqrt{\frac{R+sL}{sC}}$ is the characteristic impedance; $r = \frac{R}{h}, l = \frac{L}{h}, c = \frac{C}{h}$ are resistance, inductance, and capacitance per unit length and $h$ is the length of the line. The variables $b_k$ are referred as coefficients of the transfer function and are directly related to the moments of the transfer function [7]. Expanding the above transfer function into a Maclaurin series of $s$ around $s = 0$ leads to an infinite series, and to compute the response the series is truncated to desired order. The method of Padé approximation has been widely used to compute the response from the transfer function [9, 10]. For the case of resistive source ($R_S$) and capacitive load ($C_L$) impedances, the coefficient of $s$ in the transfer function can be obtained as [7]

$$b_1 = R_S C + R_S C_L + \frac{RC}{2} + RC_L \; . \quad (2)$$

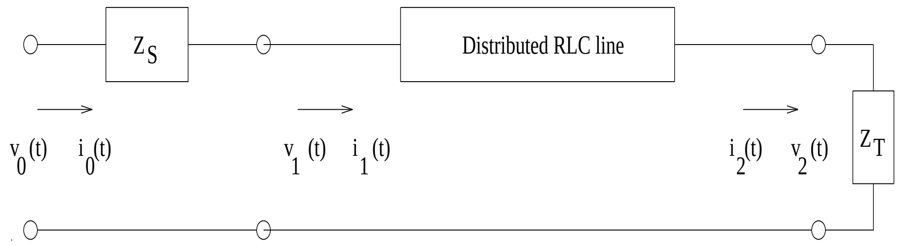


Figure 1: 2-port model of a distributed $RLC$ line with source impedance $Z_S$ and load impedance $Z_T$.

Efficient delay estimates for interconnect lines are typically derived by considering a single interconnect line with resistive source and capacitive load impedances; delay formulas for an interconnect tree come from recursive application of the formula for a single line. Elmore delay

[2] is a first order delay estimate for interconnect lines under step input. It is equal to the first moment of the system impulse response, i.e., the coefficient of $s$ or the first moment in the system transfer function $H(s)$. Applying this definition to $H(s)$ in Equation (1), the Elmore delay is equal to the coefficient $b_1$.

By considering only one pole in the transfer function, i.e, approximating the denominator polynomial to only the first moment, the single pole response can be obtained as in [13, 3]. The single pole of the transfer function is equal to the inverse of the Elmore delay $T_{ED}$. Hence, the delay at arbitrary thresholds of the single pole response can be directly related to Elmore delay (Elmore delay actually corresponds to the 63.2% threshold voltage of the single pole response). For example, delay at 50% threshold voltage is $0.69b_1$, and delay at 90% threshold voltage is $2.3b_1$. The Elmore delay estimate has been widely used as an analytical delay formula for interconnect timing analysis. However, Elmore delay cannot accurately estimate the delay for $RLC$ interconnect lines, which are the appropriate representation for interconnects whose inductive impedance[2] cannot be neglected [5]. More critically, Elmore delay cannot estimate delays when the input signal is a ramp. (Recently, [7] have developed a more accurate model analytical delay model considering the inductive effects based on the first and second moments of the transfer function. Even though their model gives accurate estimates compared to SPICE-computed delays, the model is valid only for step inputs.)

# 3 Analytical Ramp Delay Definitions

In the literature, various analytical (closed-form) delay models for step input have been proposed [2, 3, 7]. In practice, the input at any gate or root of a tree is a ramp with finite rise time, and there are no published analytical delay models for ramp input. In this section, we propose various ramp delay definitions and also compute analytical expressions for delay using the first one or two moments of the transfer function.

**Rising Ramp Input**

The finite rising ramp input shown in Figure 2 can be expressed in the time domain as

$$v_{in}(t) = \frac{V_0}{T_R}\left[tU(t) - (t - T_R)U(t - T_R)\right] \quad \text{for all } t \geq 0 \ .$$

[2] Inductive impedance is $2\pi fL$, where $f$ is the frequency of operation.

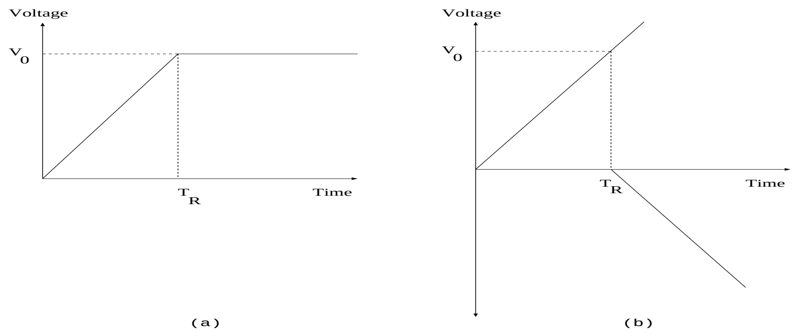


Figure 2: A ramp input function: (a) finite ramp with rise time $T_R$, and (b) finite ramp decomposed into two shifted infinite ramps.

where $U(t)$ denotes the step function. The finite ramp input in the transform domain is

$$V_{in}(s) = \frac{V_0}{T_R} \cdot \frac{1}{s^2}[1 - e^{-sT_R}]$$

In the transform domain, the output response is

$$V_R(s) = V_{in}(s)H(s) = \frac{V_0}{T_R} \cdot \frac{1}{s^2}[1 - e^{-sT_R}]H(s)$$

**Falling Ramp Input**

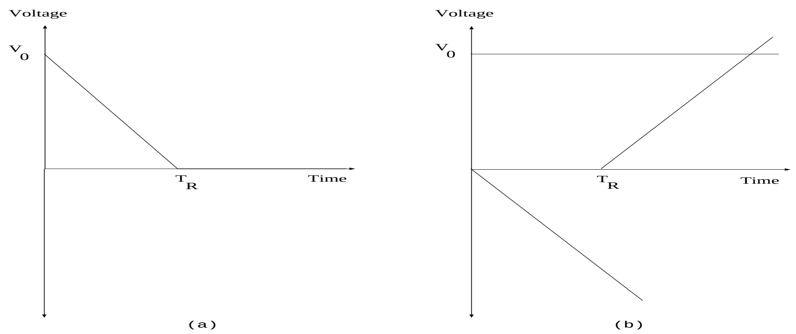


Figure 3: A ramp input function: (a) finite falling ramp with fall time $T_F$, and (b) finite falling ramp decomposed into a step input and two shifted infinite ramps.

Although we shall discuss delay models for rising ramp input only, our methodology can also be applied for falling ramp input. The finite falling ramp input can be expressed in the time domain as

$$v_{in}(t) = \frac{V_0}{T_F}\left[U(t) - tU(t) + (t - T_F)U(t - T_F)\right] \quad \text{for all } t \geq 0$$

where $U(t)$ denotes the step function (Figure 3). In the transform domain, this ramp input is

$$V_{in}(s) = \frac{V_0}{T_F}\left(\frac{T_F}{s} - \frac{1}{s^2}(1 - e^{-sT_F})\right) \ ,$$

implying that the output response $V_F(s)$ for falling ramp input can be computed by subtracting the response $V_R(s)$ for rising ramp input from the response $V_S(s)$ for step input (see [7]), i.e.,

$$\begin{aligned} V_F(s) &= \frac{V_0}{T_F}\left(\frac{T_F}{s} - \frac{1}{s^2}(1-e^{-sT_F})\right)H(s) \\ &= V_S(s) - V_R(s) \end{aligned} \tag{3}$$

Note that throughout the remainder of this paper $V_R(s)$ will be denoted as $V_{out}(s)$. We now give three distinct derivation of an analytical ramp delay estimate.

**Elmore Definition.** We may apply Elmore's original definition of delay for step input [2] to compute an analytical delay $T_{AD}$ under ramp input, i.e.,

$$\begin{aligned} T_{AD} &= \frac{1}{v_{out}(\infty)}\int_0^\infty t v'_{out}(t)dt \\ &= \frac{1}{V_0}\int_0^\infty t v'_{out}(t)dt \end{aligned} \tag{4}$$

where $v'_{out}(t)$ is the derivative of the output response under finite ramp input. Taking the Laplace transform of $v'_{out}(t)$,

$$\begin{aligned} V'_{out}(s) &= \int_0^\infty e^{-st} v'_{out}(t)dt \\ &= \int_0^\infty v'_{out}(t)dt - s\int_0^\infty t v'_{out}(t)dt + \ldots \end{aligned}$$

Equation (4) then implies that the analytical ramp input delay $T_{AD}$ in time-domain is equal to the first moment of the derivative of the response. In the transform domain, $T_{AD}$ is equal to the first moment (or coefficient of $s$) of the function $\frac{V'_{out}(s)}{V_0}$, which is equal to $s \cdot \frac{V_{out}(s)}{V_0}$. The derivative of the response in the transform domain is

$$\begin{aligned} V'_{out}(s) &= sV_{out}(s) = sV_{in}(s)H(s) \\ &= \frac{V_0}{T_R}\frac{1}{s}(1-e^{-sT_R})H(s) \\ &= \frac{V_0}{T_R}\frac{1}{s}(sT_R - \frac{s^2T_R^2}{2} + \ldots)\frac{1+a_1s+a_2s^2+....}{1+b_1s+b_2s^2+....} \\ &= V_0(1-\frac{sT_R}{2}+\ldots)\frac{1+a_1s+a_2s^2+....}{1+b_1s+b_2s^2+....} \end{aligned} \tag{5}$$

Therefore, the analytical ramp input delay is[3]

[3] A simple approximation for 90% threshold delay for ramp input, which is used in the literature so far, is equal to sum of 90% step input delay and rise time of input signal $T_R$, i.e., $T_{appx} = T_R + 2.3 * b_1$.

$$T_{AD} = \frac{T_R}{2} + b_1 - a_1 = \frac{T_R}{2} + T_{ED} \tag{6}$$

where $T_{ED}$ is the Elmore delay for a step input (i.e., the first moment of the transfer function).

**Alternative Definition of Analytical Delay.** Another definition of ramp delay from the output response is[4]

$$\begin{aligned} T_{AD} &= \frac{1}{(v_{out}(\infty) - v_{out}(0))} \int_0^\infty (v_{out}(\infty) - v_{out}(t))dt \\ &= \int_0^\infty (1 - \frac{v_{out}(t)}{V_0})dt \end{aligned} \tag{7}$$

The Laplace transform of the function $(1 - \frac{v_{out}(t)}{V_0})$ is equal to $(\frac{1}{s} - \frac{V_{out}(s)}{V_0})$, so that

$$\begin{aligned} (\frac{1}{s} - \frac{V_{out}(s)}{V_0}) &= \int_0^\infty e^{-st}(1 - \frac{v_{out}(t)}{V_0})dt \\ &= \int_0^\infty (1 - \frac{v_{out}(t)}{V_0})dt - s\int_0^\infty t(1 - \frac{v_{out}(t)}{V_0})dt + \ldots \end{aligned}$$

In the transform domain, this implies that the ramp input delay is equal to the zeroth moment (or coefficient of $s^0$) of the function $(\frac{1}{s} - \frac{V_{out}(s)}{V_0})$, i.e.,

$$T_{AD} = \lim_{s \to 0} \left[\frac{1}{s} - \frac{V_{out}(s)}{V_0}\right] \tag{8}$$

Expanding $(\frac{1}{s} - \frac{V_{out}(s)}{V_0})$ in terms of input ramp and transfer function coefficients yields

$$\begin{aligned} \left[\frac{1}{s} - \frac{V_{out}(s)}{V_0}\right] &= \left[\frac{1}{s} - \frac{1}{T_R}\frac{1}{s^2}(1 - e^{-sT_R})H(s)\right] \\ &= \frac{1}{s}\left[1 - (1 - \frac{sT_R}{2} + \ldots)\frac{1 + a_1 s + a_2 s^2 + \ldots.}{1 + b_1 s + b_2 s^2 + \ldots.}\right] \\ &= \frac{(b_1 - a_1 + \frac{T_R}{2}) + \ldots}{1 + b_1 s + b_2 s^2 + \ldots} \end{aligned} \tag{9}$$

and applying Equation (8) yields the same result

$$T_{AD} = \frac{T_R}{2} + b_1 - a_1 \tag{10}$$

**Group Delay Definition.**

The concept of group delay was initially defined for step input by Vlach et al. [15]. We now give a group delay definition for computing ramp input delay similar to that in [15], and show that it converges to same analytical expression derived in Equations (6) and (10).

[4] A similar definition is used in [8] to compute step input delay for general $RC$ networks.

Recall that *group delay* is defined as the negative of the rate of change of the phase characteristic $\phi$ of the output response $V_{out}(\omega)$ with respect to frequency, at zero frequency:

$$T_{GD} = \lim_{\omega \to 0} -\frac{\partial \phi}{\partial \omega} \ .$$

To compute the phase characteristic of the output response, we first compute the output response $V_{out}(s)$ in the transform domain and then substitute for the Laplace variable $s = j\omega$, i.e.,

$$\begin{aligned} V_{out}(\omega) &= \frac{V_0}{T_R} \cdot \frac{-1}{\omega^2}(1 - e^{-j\omega T_R}) \cdot H(\omega) \\ &= \frac{-V_0}{T_R \omega} \left[ (\frac{\omega T_R^2}{2} - \frac{\omega^3 T_R^4}{3!} + \ldots) + j(T_R - \frac{\omega^2 T_R^3}{3!} + \ldots) \right] H(\omega) \\ &= \frac{-V_0}{T_R \omega} \left[ M_1 + j M_2 \right] H(\omega) \end{aligned}$$

where $M_1$ and $M_2$ are the real and imaginary parts of the input ramp function. Writing the transfer function in terms of numerator and denominator polynomials,

$$\begin{aligned} H(\omega) &= \frac{(1 - a_2\omega^2 + \ldots) + j(a_1\omega - a_3\omega^3 + \ldots)}{(1 - b_2\omega^2 + \ldots) + j(b_1\omega - b_3\omega^3 + \ldots)} \\ &= \frac{N_1 + jN_2}{D_1 + jD_2} \end{aligned}$$

Then, the phase characteristic of the output response is

$$\phi = \tan^{-1}\frac{M_2}{M_1} + \tan^{-1}\frac{N_2}{N_1} - \tan^{-1}\frac{D_2}{D_1} \ .$$

Using

$$\frac{\partial}{\partial \omega}\left(\tan^{-1}\frac{M_2}{M_1}\right) = \frac{M_1 \frac{\partial M_2}{\partial \omega} - M_2 \frac{\partial M_1}{\partial \omega}}{M_1^2 + M_2^2}$$

we obtain the group delay

$$\begin{aligned} T_{GD} &= \lim_{\omega \to 0} -\frac{\partial \phi}{\partial \omega} \\ &= \frac{T_R}{2} + b_1 - a_1 \end{aligned} \qquad (11)$$

## 4 Single-Pole Analysis

If we approximate the system transfer function up to the first moment (or coefficient of $s$),

$$H(s) \approx \frac{1}{1 + sb_1}$$

and the output response under infinite ramp is[5]

$$\begin{aligned} U_{out}(s) &= \frac{V_0}{T_R}\frac{1}{s^2}\frac{1}{1+sb_1} \\ &= \frac{V_0}{T_R}\left[\frac{1}{s^2} - \frac{b_1}{s} + \frac{b_1}{(s+1/b_1)}\right] \end{aligned}$$

with corresponding time-domain response

$$u_{out}(t) = \frac{V_0}{T_R}\left[-b_1 + t + b_1 e^{\frac{-t}{b_1}}\right] \tag{12}$$

The time-domain response for a finite ramp is therefore

$$\begin{aligned} v_{out}(t) &= u_{out}(t) - u_{out}(t-T_R) \\ &= \frac{V_0}{T_R}\left[T_R + b_1 e^{\frac{-t}{b_1}} - b_1 e^{\frac{-(t-T_R)}{b_1}}\right] \end{aligned} \tag{13}$$

Note that as $t \to \infty$, $v_{out}(t)$ tends to a final value of $V_0$ as expected.

## 4.1 Analytical Delay Model

From the output response given in Equations (12) and (13) the analytical ramp delay can be computed using the definition in Equation (4) as

$$\begin{aligned} T_{AD} &= \frac{1}{V_0}\int_0^{T_R} t u'_{out}(t)dt + \frac{1}{V_0}\int_{T_R}^{\infty} t v'_{out}(t)dt \\ &= \frac{1}{T_R}\left[\int_0^{T_R} t dt - \int_0^{T_R} t e^{\frac{-t}{b_1}} dt - \int_{T_R}^{\infty} t e^{\frac{-t}{b_1}} dt + \int_{T_R}^{\infty} t e^{\frac{-(t-T_R)}{b_1}} dt\right] \\ &= \frac{1}{T_R}\left[\left(\frac{t^2}{2} + b_1 t e^{\frac{-t}{b_1}} + b_1^2 \frac{-t}{b_1}\right)\Big|_0^{T_R} - \left(\frac{te^{\frac{-t}{b_1}}}{-1/b_1} - \frac{e^{\frac{-t}{b_1}}}{1/b_1^2}\right)\Big|_0^{\infty} + \left(\frac{te^{\frac{-(t-T_R)}{b_1}}}{-1/b_1} - \frac{e^{\frac{-(t-T_R)}{b_1}}}{1/b_1^2}\right)\Big|_0^{\infty}\right] \\ &= \frac{T_R}{2} + b_1 \end{aligned} \tag{14}$$

**Threshold Voltage Corresponding To Analytical Ramp Delay.**

Section 2 gave three different definitions for computing an analytical ramp input delay from the output response. When the transfer function of the system is approximated up to the coefficient of $s$, this analytical delay reduces to

$$T_{AD} = \frac{T_R}{2} + b_1 \ .$$

[5] In the transform and time domains, we respectively use $U(x,s)$ and $u(x,t)$ to indicate the response for the infinite ramp input, and $V(x,s)$ and $v(x,t)$ to indicate the response for the finite ramp input.

The threshold voltage corresponding to this analytical delay is not known, and must be computed by substituting $T_{AD}$ for time in either the infinite or the finite ramp responses.

When $b_1 \ll \frac{T_R}{2}$, using the infinite ramp response in Equation (12) gives

$$\begin{aligned} u_{out}(t = T_{AD}) &= \frac{V_0}{T_R}\left[-b_1 + T_{AD} + b_1 e^{\frac{-T_{AD}}{b_1}}\right] \\ &= \frac{V_0}{2}\left[1 + \frac{2b_1}{T_R} e^{-(1+\frac{1}{2b_1/T_R})}\right] \end{aligned}$$

In the limit as $\frac{2b_1}{T_R} \rightarrow 0$ the threshold voltage reduces to $u_{out}(t = T_{AD}) = \frac{V_0}{2}$. Hence, for large rise-times or small first moment of the transfer function the analytical delay $T_{AD}$ corresponds to 50% threshold voltage.

When $b_1 \gg \frac{T_R}{2}$, using the finite ramp response in Equation (13) gives

$$\begin{aligned} v_{out}(t = T_{AD}) &= \frac{V_0}{T_R}\left[T_R + b_1 e^{\frac{-T_{AD}}{b_1}} - b_1 e^{\frac{-(T_{AD}-T_R)}{b_1}}\right] \\ &= V_0\left[1 + \frac{1}{2e}\frac{2b_1}{T_R}\left(e^{\frac{-1}{2b_1/T_R}} - e^{\frac{1}{2b_1/T_R}}\right)\right] \end{aligned}$$

In the limit as $\frac{2b_1}{T_R} \rightarrow \infty$[6] the threshold voltage reduces to $v_{out}(t = T_{AD}) = V_0(1-1/e) = 0.632V_0$. Hence, for small rise-times or large first moment of the transfer function the analytical delay $T_{AD}$ corresponds to 63.2% threshold voltage. We see that for any arbitrary values of $T_R$ and $b_1$ the threshold voltage corresponding to the analytical delay $T_{AD}$ will be between 50% and 63.2%.

## 4.2 Threshold Delay Models

**Condition for Computing Threshold Delay Using Finite or Infinite Ramp Response.**

The ramp input delay at any threshold voltage can be computed using the infinite ramp response in Equation (12) if the ramp delay is less than rise time $T_R$, or using the finite ramp response in Equation (13) if the ramp delay is greater than $T_R$. For example, the delay at threshold $Th1$ in Figure 4 is computed using the infinite ramp response, and the delay at threshold $Th2$ is computed using the finite ramp response. To determine when the infinite ramp response should be used, we write the threshold voltage corresponding to the rise-time $T_R$ in terms of interconnect and rise time parameters:

$$v_{T_R} = \frac{1}{T_R}\left[-b_1 + T_R + b_1 e^{\frac{-T_R}{b_1}}\right]$$

[6] Since $\lim_{x\rightarrow\infty} x(e^{\frac{-1}{x}} - e^{\frac{1}{x}}) = \lim_{y\rightarrow 0} \frac{(e^{-y}-e^{y})}{y} = -2$ .

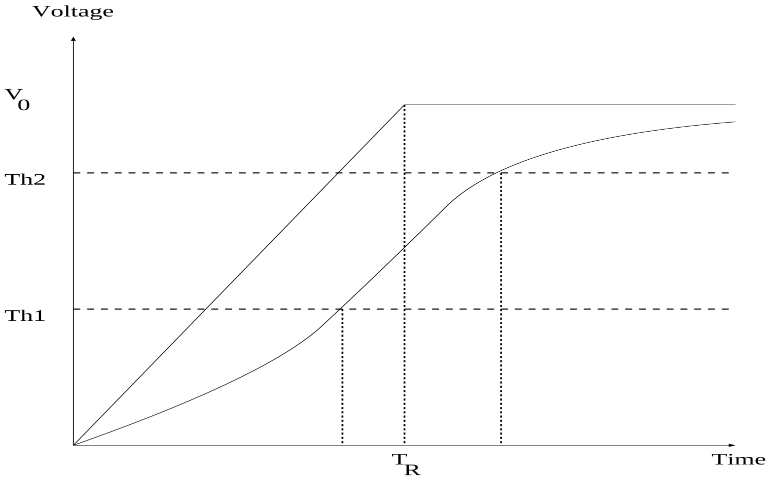


Figure 4: Ramp input delay at various threshold voltages.

$$= \left[1 - \frac{b_1}{T_R}(1 - e^{\frac{-1}{b_1/T_R}})\right] \qquad (15)$$

Here, $v_{T_R}$ is the threshold voltage at which the delay through the interconnect is equal to $T_R$. If $v_{th} \leq v_{T_R}$, delay is calculated using Equation (12), and if $v_{th} > v_{T_R}$, delay is calculated using Equation (13).

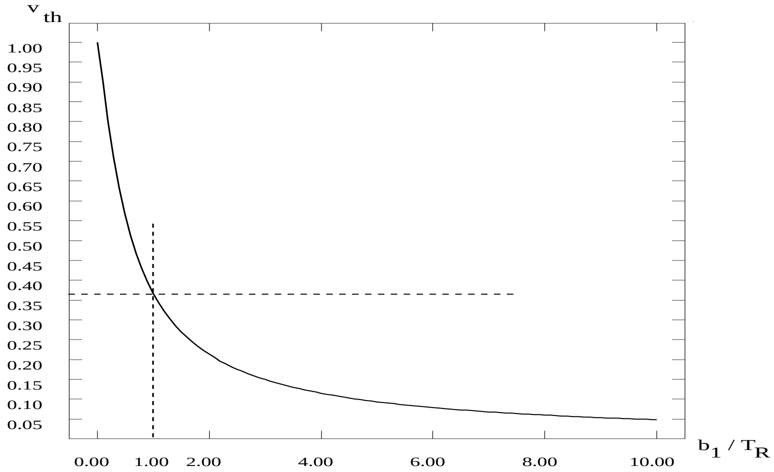


Figure 5: Variation of threshold voltage at delay equal to rise-time $T_R$ with respect to the factor $\frac{b_1}{T_R}$.

Observe that Equation (15) can be rearranged to obtain a condition on $\frac{b_1}{T_R}$ for any given threshold voltage $v_{th}$: the condition for delay calculation using infinite ramp response

$$\frac{b_1}{T_R}(1 - e^{\frac{-1}{b_1/T_R}}) \leq (1 - v_{th})$$

and the condition for delay calculation using finite ramp response is

$$\frac{b_1}{T_R}(1 - e^{\frac{-1}{b_1/T_R}}) \geq (1 - v_{th})$$

Figure 5 shows the variation of $v_{T_R}$ with respect to the factor $\frac{b_1}{T_R}$. At $b_1 = T_R$ the threshold voltage $v_{T_R}$ is $0.368V_0$, i.e., 36.8%. Since most sub-micron interconnect networks have small rise-times and large propagation delays, the delays at threshold voltages of interest (50% or 90%) will likely be computed by considering the finite ramp response as developed in Equation (17) below.[7]

**Threshold Delay Using Infinite Ramp Response.**

**Model 1.** For the infinite ramp response of Equation (12), the threshold delay is[8]

$$T_{RD1} + b_1 e^{\frac{-T_{RD1}}{b_1}} = u_{th} T_R + b_1$$

We can solve such a recursive equation in less than 10 iterations of simple back-substitution (with $T_{AD}$ as the starting value) for all the interconnect configurations we considered. Another way to evaluate the above iterative equation is by substituting some $f(T_{AD})$ for $T_{RD1}$ in the exponential term, which yields[9]

$$T_{RD1} = u_{th} T_R + b_1(1 - e^{\frac{-f(T_{AD})}{b_1}}) \,. \tag{16}$$

Here, $f(T_{AD})$ depends on the threshold voltage and $T_{AD}$. For example, for 50% threshold voltage $f(T_{AD}) = T_{AD}$ and for 90% threshold voltage $f(T_{AD}) = 2.3T_{AD}$. The delay values using Equation (16) are very close to the values obtained by solving the equation through iteration.

**Threshold Delay Using Finite Ramp Response.**

**Model 2.** For the finite ramp response of Equation (13),

$$v_{th} = \frac{1}{T_R}\left[T_R + b_1 e^{\frac{-T_{RD2}}{b_1}} - b_1 e^{\frac{-(T_{RD2}-T_R)}{b_1}}\right]$$

[7] At 50% threshold, the condition for delay calculation using infinite ramp response is $\frac{b_1}{T_R} \leq 0.625$, with delay calculated using finite ramp response otherwise. Similarly, at 90% threshold, the condition for delay calculation using infinite ramp response is $\frac{b_1}{T_R} \leq 0.1$.

[8] A simple upper bound on the delay stems from neglecting the exponential term entirely, i.e., $T_{RD1} \leq u_{th} T_R + b_1$.

[9] Again, the convention we use is that threshold delay refers to delay measured from the point when the input signal is zero. To compute delay *relative to* the input signal, subtract the corresponding threshold delay of the input signal (e.g., for 50% threshold voltage, the delay for the input ramp is $\frac{T_R}{2}$).

Collecting the threshold delay $T_{RD2}$ terms, we obtain

$$\begin{aligned} T_{RD2} &= b_1 \left| \ln \left( \frac{b_1}{T_R} \cdot \frac{(e^{\frac{1}{b_1/T_R}} - 1)}{(1 - v_{th})} \right) \right| \\ &= b_1 \left| \ln \left( \frac{F_1}{(1 - v_{th})} \right) \right| \end{aligned} \tag{17}$$

where the factor $F_1 = \frac{b_1}{T_R}(e^{\frac{1}{b_1/T_R}} - 1)$ can vary between $\infty$ and 0 as shown in Figure 6. With such a large variation in $F_1$, it is very difficult to fit the threshold delay $T_{RD2}$ against the corresponding SPICE delay.

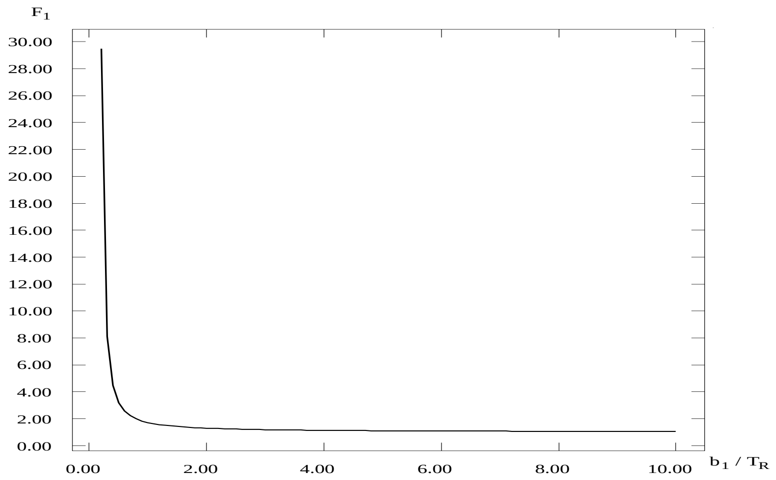


Figure 6: Variation of the factor $F_1 = \frac{b_1}{T_R}(e^{\frac{1}{b_1/T_R}} - 1)$ with respect to $\frac{b_1}{T_R}$.

**Model 3.** Since the threshold delay computed from the finite ramp response is greater than $T_R$, an alternative formula for the threshold delay can be obtained by expressing $T_{RD3}$ as

$$T_{RD3} = T_R + \tau_{RD3}$$

Substituting into Equation (13) yields

$$v_{th} = \frac{1}{T_R} \left[ T_R + b_1 e^{\frac{-T_R}{b_1}} e^{\frac{-\tau_{RD3}}{b_1}} - b_1 e^{\frac{-\tau_{RD3}}{b_1}} \right]$$

which implies

$$\tau_{RD3} = b_1 \left| \ln \left( \frac{b_1}{T_R} \cdot \frac{(1 - e^{\frac{-1}{b_1/T_R}})}{(1 - v_{th})} \right) \right| . \tag{18}$$

Therefore, the total delay is

$$T_{RD3} = T_R + b_1 \left| \ln \left( \frac{b_1}{T_R} \cdot \frac{(1 - e^{\frac{-1}{b_1/T_R}})}{(1 - v_{th})} \right) \right|$$

$$= \quad T_R + b_1 \left| \ln \left( \frac{F_2}{(1 - v_{th})} \right) \right| \qquad (19)$$

The factor $F_2 = \frac{b_1}{T_R}(1 - e^{\frac{-1}{b_1/T_R}})$ varies between 0 and 1.0 as shown in Figure 7. For $b_1 = T_R$ this factor is $F_2 = 0.632$. For $b_1 > T_R$ we can find a good approximation for $F_2$ by fitting against SPICE-computed delays, since the variation in $F_2$ values is very small. For the range of interconnect configurations studied both Model 2 and Model 3 gave essentially identical results and hence in Section 7 we report results using just Model 2 only.

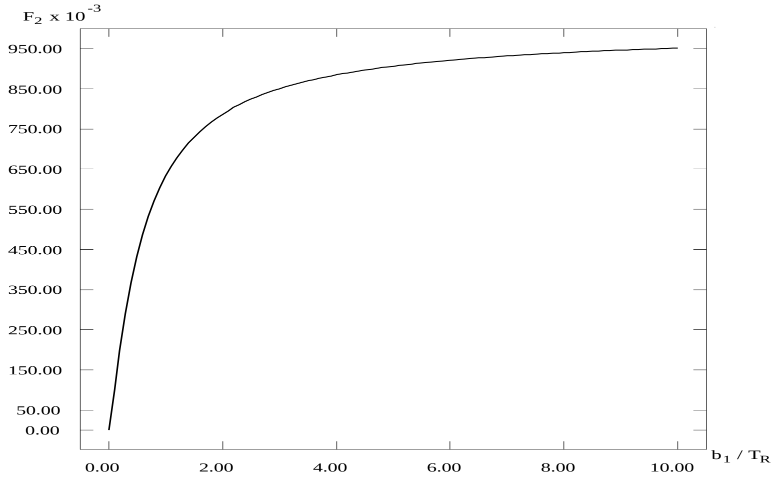


Figure 7: Variation of the factor $F_2 = \frac{b_1}{T_R}(1 - e^{\frac{-1}{b_1/T_R}})$ with respect to $\frac{b_1}{T_R}$.

# 5 Two-Pole Analysis

The two-pole methodology for interconnect response computation under step input has been discussed in [3, 17, 6]. For interconnect trees (or lines) the transfer function has a special form in which the numerator polynomial is a constant, i.e., approximating to $s^2$ term yields

$$H(s) \approx \frac{1}{1 + sb_1 + s^2 b_2} \ .$$

For the case of resistive source ($R_S$) and capacitive load ($C_L$) impedances, the transfer function coefficients are given by [7]

$$\begin{aligned} b_1 &= R_S C + R_S C_L + \frac{RC}{2} + RC_L \\ b_2 &= \frac{R_S R C^2}{6} + \frac{R_S R C C_L}{2} + \frac{(RC)^2}{24} + \frac{R^2 C C_L}{6} + \frac{LC}{2} + LC_L \end{aligned} \qquad (20)$$

For this form of the transfer function, the output response under infinite ramp input is

$$\begin{aligned} U_{out}(s) &= \frac{V_0}{T_R}\frac{1}{s^2}\frac{1}{1+sb_1+s^2b_2} \\ &= \frac{V_0}{T_R}\frac{1}{b_2s^2}\frac{1}{(s-s_1)(s-s_2)} \\ &= \frac{V_0}{T_R}\left[\frac{k_1}{s-s_1}+\frac{k_2}{s-s_2}+\frac{k_3}{s}+\frac{k_4}{s^2}\right] \end{aligned}$$

Equating the coefficients of $s$'s in numerator and denominator, we obtain the equations

$$\begin{aligned} k_1+k_2+k_3 &= 0 \\ -k_1s_2-k_2s_1-k_3(s_1+s_2)+k_4 &= 0 \\ k_3s_1s_2-k_4(s_1+s_2) &= 0 \\ k_4s_1s_2 &= \frac{1}{b_2} \\ s_1+s_2 &= \frac{-b_1}{b_2} \\ s_1s_2 &= \frac{1}{b_2} \end{aligned}$$

where $s_1$ and $s_2$ are the poles of the transfer function. Solving these six equations for the six variables, we get

$$\begin{aligned} s_1 &= \frac{-b_1+\sqrt{b_1^2-4b_2}}{2b_2} \\ s_2 &= \frac{-b_1-\sqrt{b_1^2-4b_2}}{2b_2} \\ k_1 &= \frac{b_1^2-2b_2+b_1\sqrt{b_1^2-4b_2}}{2\sqrt{b_1^2-4b_2}} = \frac{-(1+b_1s_2)}{s_1-s_2} \\ k_2 &= \frac{-b_1^2+2b_2+b_1\sqrt{b_1^2-4b_2}}{2\sqrt{b_1^2-4b_2}} = \frac{1+b_1s_1}{s_1-s_2} \\ k_3 &= -b_1 \\ k_4 &= 1 \end{aligned}$$

Substituting for these variables, the infinite ramp response in the transform domain is

$$U_{out}(s) = \frac{V_0}{T_R}\left[\frac{-b_1}{s}+\frac{1}{s^2}-\frac{1+b_1s_2}{s_1-s_2}\frac{1}{s-s_1}+\frac{1+b_1s_1}{s_1-s_2}\frac{k_2}{s-s_2}\right]$$

and the corresponding time-domain response is

$$u_{out}(t) = \frac{V_0}{T_R}\left[-b_1+t+\frac{1+b_1s_2}{s_2-s_1}e^{s_1t}+\frac{1+b_1s_1}{s_1-s_2}e^{s_2t}\right]U(t) \tag{21}$$

where $U(t)$ represents the unit step function. The time-domain response for a finite ramp is

$$\begin{aligned} v_{out}(t) &= u_{out}(t) - u_{out}(t-T_R) \\ &= \frac{V_0}{T_R}\left[T_R + \frac{1+b_1s_2}{s_2-s_1}(e^{s_1t} - e^{s_1(t-T_R)}) + \frac{1+b_1s_1}{s_1-s_2}(e^{s_2t} - e^{s_2(t-T_R)})\right]U(t) \end{aligned} \tag{22}$$

Note that the first and second moments of the transfer function can be obtained from the coefficients $b_1$ and $b_2$, i.e., $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. We use the coefficient notation $b_1, b_2$ and the moment notation $M_1, M_2$ interchangeably according to the simplicity of the expression.

**Analytical Delay Model.**

From the output response given in Equations (21) and (22), the analytical ramp delay can be computed by applying the definition in Equation (4):[10]

$$\begin{aligned} T_{AD} &= \frac{1}{V_0}\int_0^{T_R} t u'_{out}(t)dt + \frac{1}{V_0}\int_{T_R}^{\infty} t v'_{out}(t)dt \\ &= \frac{1}{T_R}\left[\int_0^{T_R} tdt + \int_0^{T_R}\frac{(1+b_1s_2)s_1}{s_2-s_1}e^{s_1t}dt + \int_0^{T_R}\frac{(1+b_1s_1)s_2}{s_1-s_2}e^{s_2t}dt\right. \\ &= \left.\int_0^{\infty} t\left(\frac{1+b_1s_2}{s_2-s_1}\right)s_1(e^{s_1t} - e^{s_1(t-T_R)})dt + \int_0^{\infty} t\left(\frac{1+b_1s_1}{s_1-s_2}\right)s_2(e^{s_2t} - e^{s_2(t-T_R)})dt\right] \\ &= \frac{T_R}{2} + b_1 \end{aligned} \tag{23}$$

This is the same expression obtained from the analytical ramp input definition in Section 3.

## 5.1 Threshold Delay Models

Depending on the sign of $b_1^2 - 4b_2$, the poles of the transfer function can be either real or complex. We now separately derive delay models from the two-pole response for each of these cases.

### 5.1.1 Real Poles

The condition for the poles to be real is $(b_1^2 - 4b_2) = (4M_2 - 3M_1^2) \geq 0$. Since the magnitude $|s_2|$ is greater than $|s_1|$, the second term in the time-domain response decreases rapidly compared to the first term. Hence, the two-pole infinite ramp response can be approximated as

$$u_{out}(t) \approx \frac{V_0}{T_R}\left[-b_1 + t + \frac{1+b_1s_2}{s_2-s_1}e^{s_1t}\right] \tag{24}$$

[10] The derivation uses the integral $\int te^{at}dt = \frac{te^{at}}{a} - \frac{e^{at}}{a^2}$.

and the finite ramp response as

$$v_{out}(t) \approx \frac{V_0}{T_R}\left[T_R + \frac{1+b_1 s_2}{s_2 - s_1}\left(e^{s_1 t} - e^{s_1(t-T_R)}\right)\right] . \tag{25}$$

Note that the residue $k_1 = \frac{1+b_1 s_2}{s_2 - s_1}$ is a positive quantity, and that the pole $s_1$ has to be negative in value for the response to converge.

**Threshold Delay for Infinite Ramp Response.**

**Model 4.** The delay $T_{RD4}$ at threshold voltage $u_{th}$ can be obtained as

$$T_{RD4} + \frac{1+b_1 s_2}{s_2 - s_1} e^{s_1 T_{RD4}} = u_{th} T_R + b_1$$

Again, we were able to solve the above equation in less than 10 iterations for the interconnect configurations we considered. Another way to evaluate the above iterative equation is by substituting some $f(T_{AD})$ for $T_{RD4}$ in the exponential term, which yields

$$T_{RD4} = u_{th} T_R + b_1 - \frac{1+b_1 s_2}{s_2 - s_1} e^{s_1 f(T_{AD})} \tag{26}$$

where $f(T_{AD})$ depends on the threshold voltage and $T_{AD}$. For example, for 50% threshold voltage $f(T_{AD}) = T_{AD}$ and for 90% threshold voltage $f(T_{AD}) = 2.3 T_{AD}$. The delay values using Equation (16) are very close to the values obtained by solving the equation through iteration.

**Threshold Delay for Finite Ramp Response.**

**Model 5.** The delay $T_{RD5}$ at threshold voltage $v_{th}$ can be obtained from the response as

$$v_{th} T_R = T_R - \frac{1+b_1 s_2}{s_2 - s_1}(e^{-s_1 T_R} - 1) e^{s_1 T_{RD5}}$$

Since the value of the pole $s_1$ is negative, the quantity $(e^{-s_1 T_R} - 1)$ is positive and the residue $\frac{1+b_1 s_2}{s_2 - s_1}$ is also positive. Thus, the delay expression reduces to

$$\begin{aligned} T_{RD5} &= \frac{1}{|s_1|}\left|\ln\left(\frac{(1+b_1 s_2)(e^{|s_1|T_R} - 1)}{(s_2 - s_1) T_R (1 - v_{th})}\right)\right| \\ &= \frac{1}{|s_1|}\left|\ln\left(\frac{F_3}{(1 - v_{th})}\right)\right| \end{aligned} \tag{27}$$

where the factor $F_3 = \frac{(1+b_1 s_2)(e^{|s_1|T_R} - 1)}{(s_2 - s_1) T_R}$ can vary widely.

**Model 6.** Since the threshold delay computed from the finite ramp response is greater than $T_R$, an alternative formula for the threshold delay can be obtained by assuming the form

$$T_{RD6} = T_R + \tau_{RD6}$$

Substituting into Equation (25) yields

$$v_{th}T_R = T_R - \frac{1+b_1s_2}{s_2-s_1}(1-e^{s_1T_R})e^{s_1\tau_{RD6}}$$

which implies

$$\begin{aligned}\tau_{RD6} &= \frac{1}{|s_1|}\left|\ln\left(\frac{(1+b_1s_2)(1-e^{-|s_1|T_R})}{(s_2-s_1)T_R(1-v_{th})}\right)\right| \\ &= \frac{1}{|s_1|}\left|\ln\left(\frac{F_4}{(1-v_{th})}\right)\right| \qquad (28)\end{aligned}$$

where the factor $F_4 = \frac{(1+b_1s_2)(1-e^{-|s_1|T_R})}{T_R(s_2-s_1)}$ varies over only a small range. The delay is

$$T_{RD6} = T_R + \frac{1}{|s_1|}\left|\ln\left(\frac{F_4}{(1-v_{th})}\right)\right| \ . \qquad (29)$$

For the range of interconnect configurations studied both Model 5 and Model 6 gave essentially identical results and hence in Section 7 we report results using just Model 5 only.

### 5.1.2 Complex Poles

The condition for complex poles is $(4M_2 - 3M_1^2) = (b_1^2 - 4b_2) \leq 0$. Even though for most cases of interest the poles turn out to be real (see Section 7), here we present analytical delay models for the case of complex poles. Even for complex poles, the response for infinite and finite ramp inputs can be calculated from the expressions in Equations (21) and (22). We can write the poles in the form $s_1 = -\alpha + \jmath\beta$ and $s_2 = -\alpha - \jmath\beta$, so that the infinite ramp response is

$$\begin{aligned}u_{out}(t) &= \frac{V_0}{T_R}\left[-b_1 + t + \frac{1+b_1s_2}{s_2-s_1}e^{s_1t} + \frac{1+b_1s_1}{s_1-s_2}e^{s_2t}\right] \\ &= \frac{V_0}{T_R}\left[-b_1 + t + \frac{b_1\beta + \jmath(1-\alpha b_1)}{2\beta}e^{(-\alpha+\jmath\beta)t} + \frac{b_1\beta - \jmath(1-\alpha b_1)}{2\beta}e^{(-\alpha-\jmath\beta)t}\right] \\ &= \frac{V_0}{T_R}\left[-b_1 + t + e^{-\alpha t}\left(b_1\cos(\beta t) - \frac{(1-\alpha b_1)}{\beta}\sin(\beta t)\right)\right] \\ &= \frac{V_0}{T_R}\left[-b_1 + t + \left(\frac{\sqrt{1-2\alpha b_1 + b_1^2(\alpha^2+\beta^2)}}{\beta}\right)e^{-\alpha t}\sin(\beta t - \rho)\right] \\ &= \frac{V_0}{T_R}\left[-b_1 + t + \frac{e^{-\alpha t}}{\beta}\sin(\beta t - \rho)\right] \qquad (30)\end{aligned}$$

where

$$\rho = \tan^{-1}\left(\frac{b_1\beta}{1-b_1\alpha}\right) \ ; \quad \alpha = \frac{b_1}{2b_2} = \frac{M_1}{2(M_1^2 - M_2)} \ ; \quad \beta = \frac{\sqrt{4b_2 - b_1^2}}{2b_2} = \frac{\sqrt{3M_1^2 - 4M_2}}{2(M_1^2 - M_2)}$$

Similarly, the finite ramp response can be obtained as

$$v_{out}(t) = \frac{V_0}{T_R}\left[T_R + \frac{1}{\beta}\left(e^{-\alpha t}\sin(\beta t - \rho) - e^{-\alpha(t-T_R)}\sin(\beta(t-T_R)-\rho)\right)\right] \tag{31}$$

**Threshold Delay for Infinite Ramp Response.**

The delay at a given threshold voltage can be computed by solving for time recursively in Equation (30), i.e.,

$$e^{-\alpha t}\sin(\beta t - \rho) = \beta(u_{th}T_R + b_1 - t) \tag{32}$$

**Model 7.** One way to solve the recursive Equation (32) is to approximate the sine variable by the first term of the Taylor series, i.e.,

$$e^{-\alpha t}\frac{\beta(u_{th}T_R + b_1 - t)}{(\beta t - \rho)}$$

which yields

$$T_{RD7} = \frac{1}{\alpha}\left|\ln\left(\frac{\beta T_{RD7} - \rho}{\beta(u_{th}T_R + b_1 - T_{RD7})}\right)\right| \tag{33}$$

Even though this equation is still recursive, we can now approximate the delay $T_{RD7}$ in the logarithmic expression with either a function of analytical delay $f(T_{AD})$, or the factor $F_5 = \left|\ln\left(\frac{\beta T_{RD7}-\rho}{\beta(u_{th}T_R+b_1-T_{RD7})}\right)\right|$ can be approximated by a constant for the required range of interconnect parameters by fitting against SPICE delays.

**Model 8.** Another way to solve the recursive Equation (32) is to approximate the time variable in the exponential term by a function of the analytical delay expression, i.e., $f(T_{AD})$ is used as an approximation for the time variable $t$ in the exponential term. Expanding sine as a Taylor series and considering only the first term yields

$$T_{RD8} = \left(\frac{(u_{th}T_R + b_1)e^{\alpha f(T_{AD})} + \frac{\rho}{\beta}}{(1 + e^{\alpha f(T_{AD})})}\right) \tag{34}$$

**Model 9.** If $\alpha t$ in the exponential term of Equation (32) is $O(1)$, it cannot be expanded as a Taylor series because the series becomes divergent. However, if we express the exponential term as $e^{(\alpha t - 1)}$ and then expand as a Taylor series, we get

$$\begin{aligned}
(u_{th}T_R + b_1 - T_{RD9})e^{\alpha T_{RD9}} &= \frac{1}{\beta}\sin(\beta T_{RD9} - \rho) \\
(u_{th}T_R + b_1 - T_{RD9})e^{(\alpha T_{RD9} - 1)} &= \frac{1}{e}(T_{RD9} - \frac{\rho}{\beta}) \\
e\alpha T_{RD9}^2 + T_{RD9}(1 - e\alpha(u_{th}T_R + b_1)) - \frac{\rho}{\beta} &= 0
\end{aligned}$$

Solving the above quadratic equation we obtain two solutions for delay; the feasible one is

$$T_{RD9} = \frac{-(1 - e\alpha(u_{th}T_R + b_1)) + \sqrt{(1 - e\alpha(u_{th}T_r + b_1))^2 + \frac{4e\alpha\rho}{\beta}}}{2e\alpha} \tag{35}$$

**Threshold Delay for Finite Ramp Response.**

The delay at a given threshold voltage can be computed by solving for time in Equation (31) recursively, i.e.,

$$\left(e^{-\alpha(t-T_R)} \sin(\beta(t - T_R) - \rho) - e^{-\alpha t} \sin(\beta t - \rho)\right) = T_R\beta(1 - v_{th}) \tag{36}$$

**Model 10.** Again we approximate the sine variable in Equation (36) by the first term of the Taylor series, which yields

$$\left(e^{-\alpha(t-T_R)}(\beta(t - T_R) - \rho) - e^{-\alpha t}(\beta t - \rho)\right) = T_R\beta(1 - v_{th})$$

The threshold delay can be obtained as

$$T_{RD10} = \frac{1}{\alpha}\left|\ln\left(\frac{(\beta T_{RD10} - \rho)(e^{\alpha T_R} - 1) - \beta T_R e^{\alpha T_R}}{\beta T_R(1 - v_{th})}\right)\right| \tag{37}$$

**Model 11.** Again, an alternative delay model approximates the time variable in the exponential term of Equation (36) by the analytical delay expression derived in the previous sections, i.e., $T_{RD11}$ is replaced by $T_{AD}$ in the exponential terms. This yields

$$T_{RD11} = \left(\frac{(1 - v_{th})T_R e^{\alpha f(T_{AD})} + T_R e^{\alpha T_R} + \frac{\rho}{\beta}(e^{\alpha T_R} - 1)}{(e^{\alpha T_R} - 1)}\right) \tag{38}$$

**Model 12.** And again, if we assume $\alpha t$ is $O(1)$ in the exponential term of Equation (32), it cannot be expanded as a Taylor series. Expressing the exponential term as $e^{(\alpha t - 1)}$ and then expanding as a Taylor series, we get

$$\begin{aligned}
\left(e^{-\alpha t} \sin(\beta t - \rho) - e^{-\alpha(t-T_R)} \sin(\beta(t - T_R) - \rho)\right) &= -T_R\beta(1 - v_{th}) \\
\left(-\alpha T_{RD12}(\beta T_{RD12} - \rho) + \alpha T_{RD12} e^{\alpha T_R}(\beta(T_{RD12} - T_R) - \rho)\right) &= -\frac{T_R}{e}\beta(1 - v_{th}) \\
\alpha\beta(e^{\alpha T_R} - 1)T_{RD12}^2 - (\alpha\rho(e^{\alpha T_R} - 1) + \alpha\beta T_R e^{\alpha T_R})T_{RD12} + \frac{T_R}{e}\beta(1 - v_{th}) &= 0
\end{aligned}$$

The feasible solution for delay is

$$T_{RD12} = \frac{(\alpha\rho(e^{\alpha T_R} - 1) + \alpha\beta T_R e^{\alpha T_R}) + \sqrt{(\alpha\rho(e^{\alpha T_R} - 1) + \alpha\beta T_R e^{\alpha T_R})^2 - \frac{4}{e}T_R\alpha\beta^2(e^{\alpha T_R} - 1)(1 - v_{th})}}{2\alpha\beta(e^{\alpha T_R} - 1)} \tag{39}$$

## 6 Interconnection Trees

Finally, we describe how to extend our analytical models to estimate delays in arbitrary interconnect trees. An $RLC$ network is called an $RLC$ *tree* if it does not contain a closed path of resistors and inductors, i.e., all resistors and inductors are floating with respect to ground, and all capacitors are connected to ground. Consider an $RLC$ interconnect tree with root (or source) $S$ and set of sinks (or leaves) $\{1, 2, \ldots, n\}$. The unique path from root $S$ to the sink node $i$ is denoted by $p(i)$ and is referred as the *main path*. The edges/nodes not on the main path are referred as the *off-path* edges/nodes. We model each edge on the main path of the tree using a lumped $RLC$ segment, e.g., an **L**, **T**, or **Π** model.[11]

We approximate the off-path subtree rooted at node $i$ with its admittance. At any node $i$, the admittance $Y_i$ is equal to (i) the capacitance of node $i$ ($C_i$) if there is no subtree at node $i$, or (ii) to the sum of the capacitance of node $i$ ($C_i$) and the subtree admittance $Y_{T(i)}$ otherwise. In other words,

$$Y_i \begin{array}{lll} = & sC_i & \text{if node } i \text{ has no off-path subtree} \\ = & sC_i + Y_{T(i)} & \text{if node } i \text{ has an off-path subtree} \end{array}$$

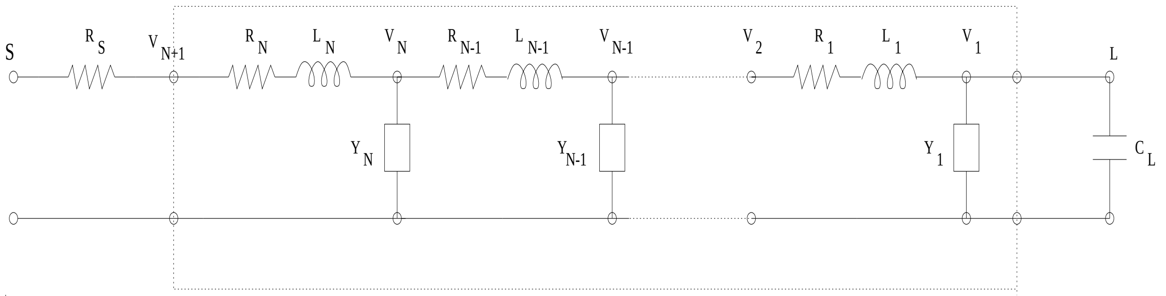


Figure 8: Representation of the main path in the tree, where each distributed line is modeled using $RLC$ segments. $Y_i$ indicates the off-path subtree admittance at node $i$.

With this approximation, the main path reduces to an $RLY$ equivalent circuit. Only two admittance moments need to be computed for an exact transfer function moment computation for the main path. The $k^{th}$ coefficient $b_k$ of the transfer function for the general $RLY$ circuit of Figure 8 can be obtained using the recursion equation given in [6]. The first and second

[11]Our model is not limited to traditional segment models, and accuracy of our results would likely improve if we use non-uniform segment models [6, 16] designed to perfectly match the low-order moments of the distributed $RLC$ line.

coefficients of the transfer function are

$$
\begin{aligned}
b_1^{SL} &= R_S \sum_{j=1}^{N} Y_{1,j} + R_N \sum_{j=1}^{N} Y_{1,j} + b_1^N \\
b_2^{SL} &= R_S \sum_{j=1}^{N} Y_{1,j} \cdot b_1^j + R_S \sum_{j=1}^{N} Y_{2,j} + R_N \sum_{j=1}^{N} Y_{1,j} \cdot b_1^j + R_N \sum_{j=1}^{N} Y_{2,j} + L_N \sum_{j=1}^{N} Y_{1,j} + b_2^N
\end{aligned} \quad (40)
$$

The first and second moments are expressed in terms of coefficients as $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. For any given source-sink pair the coefficients $b_1$ and $b_2$ can be computed in linear time by traversing the main path and using the Equation (40) to obtain transfer function coefficients.

# 7 Experimental Results

We evaluate the above models by simulating various $RLC$ interconnect lines with different source/load impedances and different input rise times. We consider typical interconnect parameters encountered in single-chip interconnects [7], with the length of the interconnect being 2000 $\mu m$. The source resistance is varied between 100 to 1000 $\Omega$ and the load capacitance is varied from 0.1 to 1.0 $pf$. We also consider 100 $ps$ and 500 $ps$ rise times for the input ramp.

For all our experiments, we compute exact 50% and 90% delays from the response at the load using the SPICE3e simulator. The step input delay is computed using the Elmore delay formula and then multiplying it with the appropriate constant for the given threshold voltage. For example, Elmore delay at 50% threshold voltage is $0.69b_1$ and at 90% threshold voltage is $2.3b_1$. We also find that Elmore delay as a bound, which corresponds to $T_{AD} = \frac{T_R}{2} + b_1$ from the paper [4], is not at all close to SPICE-computed 50% threshold delays and, and deviates as much as 100% from the SPICE-computed delays. Also, increased rise time of the input signal deviates the Elmore delay further from SPICE-computed delays (see Tables 1 and 3).

For a comparison, we also present delay estimates using the analytical ramp delay model $T_{AD}$. When the rise time of the ramp input is increased from 100 $ps$ to 500 $ps$ the SPICE delays at 50% threshold are increased by approximately 200 $ps$, which suggests that delay at 50% threshold voltage is proportional to $\frac{T_R}{2}$. This effect of the rise time is well modeled in the analytical ramp delay model $T_{AD}$. Figures 9 and 10 show that the response computed from single-pole model, and two-pole model for the first case in Tables 1 and 3 are identical to the SPICE response. To computed ramp input delays using the single-pole methodology we used either the Model 1 or

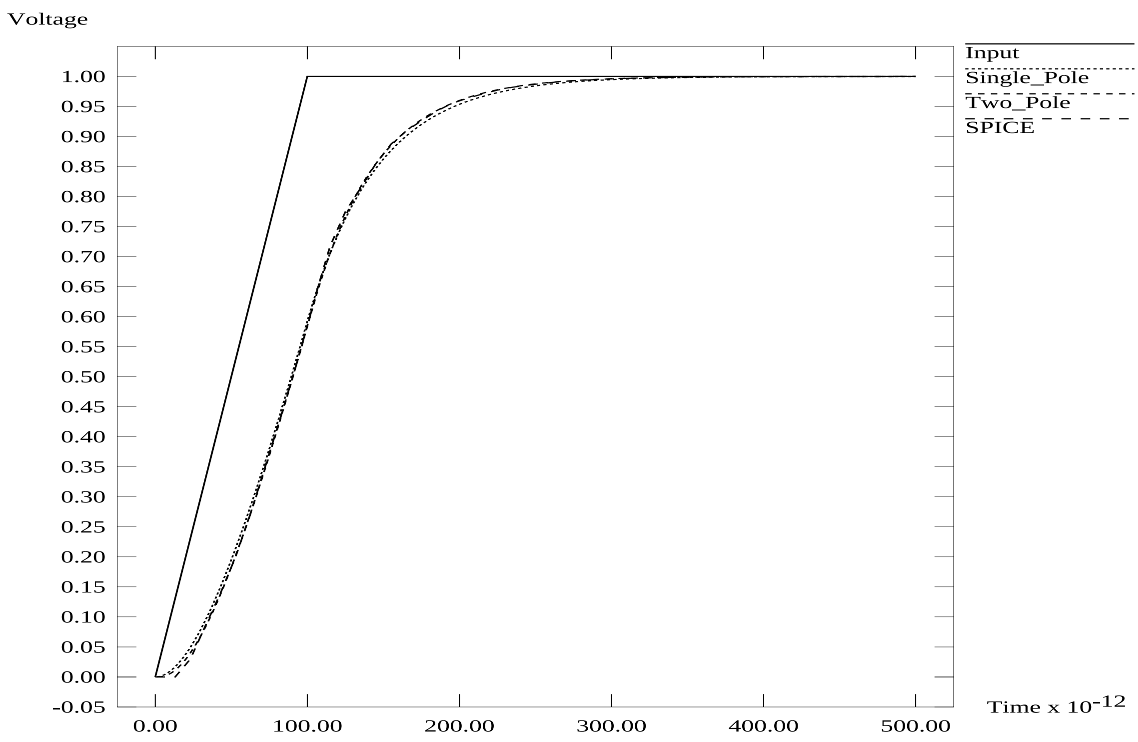


Figure 9: Response due to SPICE, single-pole model, and two-pole model for the first case in Table 1. The rise-time of the ramp input is 100 $ps$.

Model 2, depending on the value of the first moment $b_1$ and the threshold voltage of interest. Similarly, to compute ramp input delays using the two-pole methodology we use either Model 4 or Model 5, again depending on the value of $b_1$ and the threshold voltage of interest. (If the delay is computed using the infinite ramp response then we mark those delays in the Table with (*)). Tables 1 and 2 gives 50% and 90% delay estimates for ramp input with 100 $ps$ rise time. Tables 3 and 4 gives 50% and 90% delay estimates for ramp input with 500 $ps$ rise time. Over our range of test cases, Elmore delay estimates can be as much as 100% away from the SPICE-computed delays and are underestimating. In contrast, our single-pole delay estimates are within 4% of SPICE delays and the two-pole delay estimates are within 2.3% of SPICE delays.

# 8 Conclusions

Fast delay estimation methods, as opposed to simulation techniques, are needed for incremental performance-driven layout synthesis. Estimation methods based on Elmore delay for a step

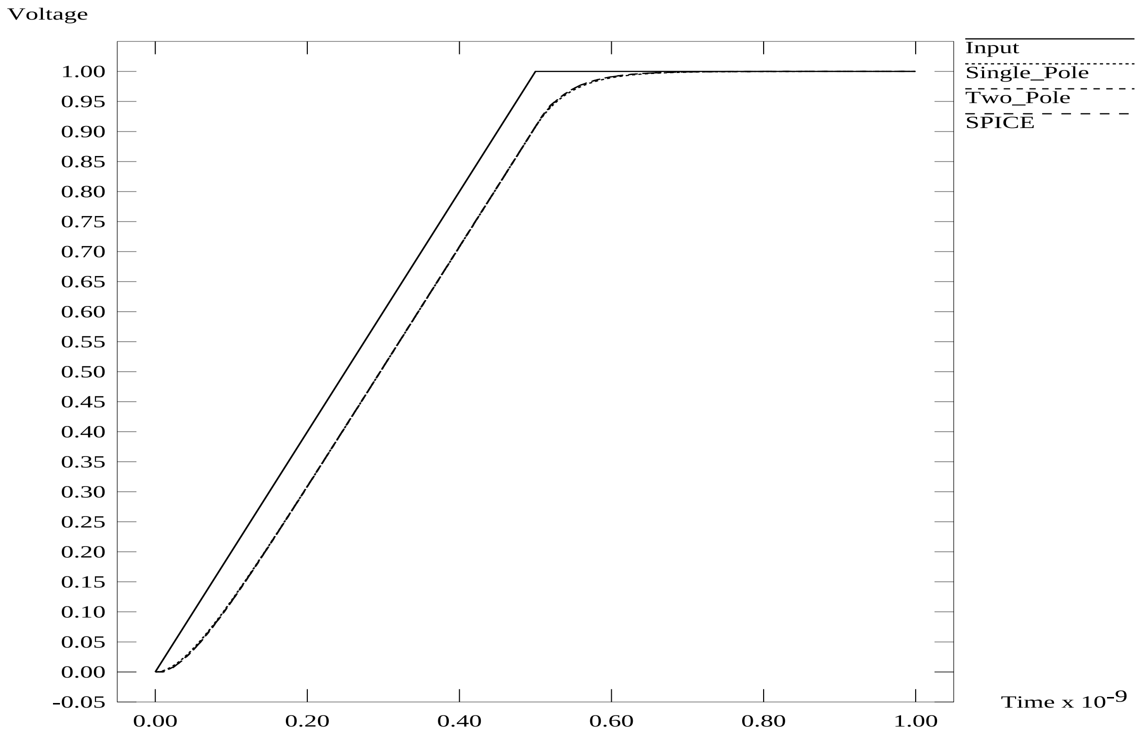


Figure 10: Response due to SPICE, single-pole model, and two-pole model for the first case in Table 3. The rise-time of the ramp input is 500 $ps$.

input, although efficient, cannot accurately estimate the delay for $RLC$ interconnect lines. We have obtained new analytical delay models under ramp input, based on the first and second moments of $RLC$ interconnection lines. Resulting delay estimates are significantly more accurate than Elmore delay estimates. We also describe how to extend our delay models to estimate source-sink delays in arbitrary interconnect trees.

| Interconnect parameters | Driver Res. | Load Cap. | Delay from Response | Elmore Delay | Analytical Delay | Single-Pole Delay | Two-Pole Delay |
|---|---|---|---|---|---|---|---|
| **r, l, c** | $\mathbf{R_S}$ | $\mathbf{C_T}$ | **SPICE** | $\mathbf{0.693b_1}$ | $\mathbf{T_{AD}}$ | **Model 1/2** | **Model 4/5** |
| $/\mu m$ | $\Omega$ | $pf$ | $ps$ | $ps$ | $ps$ | $ps$ | $ps$ |
| $r = 0.0015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 83.41 | 25.48 | 86.76 | 83.29* | 83.90* |
| " | 500 | 0.01 | 178.14 | 125.85 | 231.56 | 178.14 | 178.36 |
| " | 1000 | 0.01 | 302.08 | 251.31 | 412.56 | 302.45 | 302.59 |
| " | 100 | 0.1 | 90.40 | 31.90 | 96.03 | 90.31* | 92.49* |
| " | 500 | 0.1 | 209.13 | 157.19 | 276.83 | 209.06 | 209.33 |
| " | 1000 | 0.1 | 364.29 | 313.81 | 502.83 | 364.80 | 364.97 |
| " | 100 | 1 | 150.40 | 96.14 | 188.73 | 149.15 | 150.80 |
| " | 500 | 1 | 521.76 | 470.91 | 729.53 | 521.63 | 522.02 |
| " | 1000 | 1 | 989.25 | 939.38 | 1405.53 | 989.89 | 990.15 |
| $r = 0.015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 87.30 | 28.96 | 91.78 | 87.14* | 88.14* |
| " | 500 | 0.01 | 181.26 | 129.33 | 236.58 | 181.56 | 182.32 |
| " | 1000 | 0.01 | 304.81 | 254.79 | 417.58 | 305.92 | 306.58 |
| " | 100 | 0.1 | 95.71 | 37.06 | 103.48 | 95.76* | 97.19* |
| " | 500 | 0.1 | 213.95 | 162.36 | 284.28 | 214.17 | 215.17 |
| " | 1000 | 0.1 | 368.92 | 318.97 | 510.28 | 369.95 | 370.83 |
| " | 100 | 1 | 171.69 | 118.14 | 220.48 | 170.60 | 173.20 |
| " | 500 | 1 | 542.82 | 492.91 | 761.28 | 543.61 | 545.19 |
| " | 1000 | 1 | 1009.78 | 961.38 | 1437.28 | 1011.89 | 1013.35 |

Table 1: The length of the interconnect line in these experiments is always $h = 2000\ \mu m$. The rise time of the input ramp is 100 $ps$. The delay estimates refer to 50% threshold voltage. (*) indicates that the delay is computed using the infinite ramp response models.

| Interconnect parameters r, l, c $/\mu m$ | Driver Res. $R_S$ $\Omega$ | Load Cap. $C_T$ $pf$ | Delay from Response SPICE $ps$ | Elmore Delay $2.3b_1$ $ps$ | Analytical Delay $T_{AD}$ $ps$ | Single-Pole Delay Model 1/2 $ps$ | Two-Pole Delay Model 4/5 $ps$ |
|---|---|---|---|---|---|---|---|
| $r = 0.0015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 141.45 | 84.64 | 86.76 | 145.35 | 142.51 |
| " | 500 | 0.01 | 468.31 | 481.05 | 231.56 | 470.34 | 469.45 |
| " | 1000 | 0.01 | 882.02 | 834.82 | 412.56 | 885.97 | 885.40 |
| " | 100 | 0.1 | 160.80 | 105.86 | 96.03 | 164.70 | 161.00 |
| " | 500 | 0.1 | 571.76 | 521.70 | 276.83 | 574.12 | 573.02 |
| " | 1000 | 0.1 | 1089.60 | 1041.50 | 502.83 | 1093.60 | 1092.84 |
| " | 100 | 1 | 366.41 | 319.07 | 188.73 | 372.42 | 366.41 |
| " | 500 | 1 | 1611.96 | 1562.91 | 729.53 | 1615.28 | 1613.61 |
| " | 1000 | 1 | 3166.78 | 3117.71 | 1405.53 | 3171.53 | 3170.40 |
| $r = 0.015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 150.46 | 96.20 | 91.78 | 155.74 | 151.32 |
| " | 500 | 0.01 | 475.58 | 429.62 | 236.58 | 481.84 | 478.83 |
| " | 1000 | 0.01 | 888.90 | 846.38 | 417.58 | 897.52 | 894.79 |
| " | 100 | 0.1 | 173.70 | 123.00 | 103.48 | 180.72 | 174.79 |
| " | 500 | 0.1 | 583.34 | 538.84 | 284.28 | 591.23 | 587.22 |
| " | 1000 | 0.1 | 1100.31 | 1058.64 | 510.28 | 1110.74 | 1107.07 |
| " | 100 | 1 | 429.38 | 392.10 | 220.48 | 444.98 | 435.47 |
| " | 500 | 1 | 1667.70 | 1635.94 | 761.28 | 1688.37 | 1681.78 |
| " | 1000 | 1 | 3217.53 | 3190.74 | 1437.28 | 3244.63 | 3238.48 |

Table 2: The length of the interconnect line in these experiments is always $h = 2000\ \mu m$. The rise time of the input ramp is 100 $ps$. The delay estimates refer to 90% threshold voltage.

| Interconnect parameters r,l,c $/\mu m$ | Driver Res. $R_S$ $\Omega$ | Load Cap. $C_T$ $pf$ | Delay from Response SPICE $ps$ | Elmore Delay $0.693b_1$ $ps$ | Analytical Delay $T_{AD}$ $ps$ | Single-Pole Delay Model 1/2 $ps$ | Two-Pole Delay Model 4/5 $ps$ |
|---|---|---|---|---|---|---|---|
| $r = 0.0015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 286.69 | 25.48 | 286.76 | 286.74* | 286.75* |
| " | 500 | 0.01 | 412.74 | 125.85 | 431.56 | 414.70* | 414.86* |
| " | 1000 | 0.01 | 529.27 | 251.31 | 612.56 | 529.60 | 529.76 |
| " | 100 | 0.1 | 295.89 | 31.89 | 296.03 | 295.95* | 295.98* |
| " | 500 | 0.1 | 444.89 | 157.19 | 476.83 | 444.93* | 449.33* |
| " | 1000 | 0.1 | 586.18 | 313.81 | 702.83 | 586.65 | 586.84 |
| " | 100 | 1 | 380.47 | 96.14 | 388.73 | 380.31* | 381.10* |
| " | 500 | 1 | 736.28 | 470.91 | 929.53 | 736.27 | 736.70 |
| " | 1000 | 1 | 1196.70 | 939.38 | 1605.53 | 1197.26 | 1197.53 |
| $r = 0.015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 291.26 | 28.96 | 291.78 | 291.74* | 291.76* |
| " | 500 | 0.01 | 416.17 | 129.33 | 436.58 | 418.61* | 419.13* |
| " | 1000 | 0.01 | 531.97 | 254.79 | 617,58 | 532.70 | 533.51 |
| " | 100 | 0.1 | 302.76 | 37.06 | 303.48 | 303.30* | 303.38* |
| " | 500 | 0.1 | 449.92 | 162.36 | 484.28 | 454.63* | 455.44* |
| " | 1000 | 0.1 | 590.66 | 318.97 | 710.28 | 591.45 | 592.47 |
| " | 100 | 1 | 404.93 | 118.14 | 420.48 | 406.01* | 407.54* |
| " | 500 | 1 | 756.92 | 492.91 | 961.28 | 757.61 | 759.29 |
| " | 1000 | 1 | 1217.00 | 961.39 | 1637.28 | 1219.09 | 1220.57 |

Table 3: The length of the interconnect line in these experiments is always $h = 2000\ \mu m$. The rise time of the input ramp is 500 $ps$. The delay estimates refer to 50% threshold voltage. (*) indicates that the delay is computed using infinite ramp response models.

| Interconnect parameters r, l, c $/\mu m$ | Driver Res. $R_S$ $\Omega$ | Load Cap. $C_T$ $pf$ | Delay from Response SPICE $ps$ | Elmore Delay $2.3b_1$ $ps$ | Analytical Delay $T_{AD}$ $ps$ | Single-Pole Delay Model 1/2 $ps$ | Two-Pole Delay Model 4/5 $ps$ |
|---|---|---|---|---|---|---|---|
| $r = 0.0015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 486.68 | 84.64 | 286.76 | 486.76* | 486.76* |
| " | 500 | 0.01 | 720.32 | 481.05 | 431.56 | 722.18 | 721.47 |
| " | 1000 | 0.01 | 1109.57 | 834.82 | 612.56 | 1113.11 | 1112.57 |
| " | 100 | 0.1 | 495.91 | 105.86 | 296.03 | 496.03* | 496.03* |
| " | 500 | 0.1 | 814.22 | 521.70 | 476.83 | 816.49 | 815.53 |
| " | 1000 | 0.1 | 1311.62 | 1041.50 | 702.83 | 1315.45 | 1314.76 |
| " | 100 | 1 | 633.35 | 319.07 | 388.73 | 637.74 | 633.63 |
| " | 500 | 1 | 1826.42 | 1562.91 | 929.53 | 1829.93 | 1828.28 |
| " | 1000 | 1 | 3374.25 | 3117.71 | 1605.53 | 3378.89 | 3377.78 |
| $r = 0.015\ \Omega$ $c = 0.176\ ff$ $l = 0.246\ ph$ | 100 | 0.01 | 491.19 | 96.20 | 291.78 | 491.78* | 491.78* |
| " | 500 | 0.01 | 727.03 | 429.62 | 436.58 | 732.44 | 730.00 |
| " | 1000 | 0.01 | 1115.99 | 846.38 | 617.58 | 1124.30 | 1121.72 |
| " | 100 | 0.1 | 502.72 | 123.00 | 303.48 | 503.59 | 503.84 |
| " | 500 | 0.1 | 825.17 | 538.84 | 484.28 | 832.34 | 832.84 |
| " | 1000 | 0.1 | 1322.06 | 1058.64 | 710.28 | 1332.25 | 1328.71 |
| " | 100 | 1 | 686.70 | 392.10 | 420.48 | 699.78 | 692.47 |
| " | 500 | 1 | 1881.85 | 1635.64 | 961.28 | 1902.37 | 1895.88 |
| " | 1000 | 1 | 3424.77 | 3190.74 | 1637.28 | 3451.83 | 3445.71 |

Table 4: The length of the interconnect line in these experiments is always $h = 2000\ \mu m$. The rise time of the input ramp is 500 $ps$. The delay estimates refer to 90% threshold voltage.

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